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(54) MOS system and methods of use

(57) The use of single doping type and/or intrinsic silicon in realization of Schottky barrier junction based single device inverting and single device non-inverting systems which demonstrate operational characteristics similar to multiple device (CMOS) systems, is disclosed. Variations of said single device inverting and single device non-inverting systems can be operated as modulators, nonlatching (SCR's) and/or gate voltage controlled direction of rectification devices. Source Coupled Regeneratively Switching Schottky barrier CMOS device systems comprising seriesed N-Channel and P-Channel MOSFETS, are also disclosed. Self-delineating device fabrication procedures for realizing Schottky barrier MOSFETS with leakage current limiting Schottky barrier junctions only at the ends of semiconductor channel regions, are further disclosed. Presented are experimentally obtained results which demonstrate operational characteristics of P and N-Channel Schottky barrier MOSFET devices fabricated by a disclosed fabrication procedure in which chromium was used as a Schottky barrier silicide forming metal. The present invention promises to increase packing density in CMOS circuitry by at least one-third and offers increased speed of operation inherrant with Schottky barrier junctions.

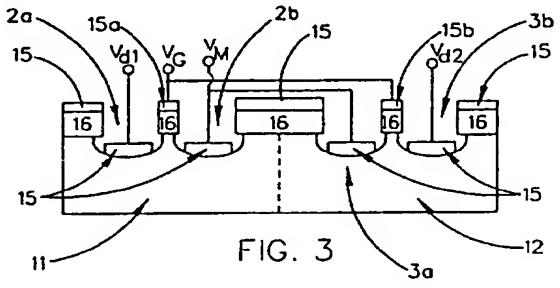

FIG. 3

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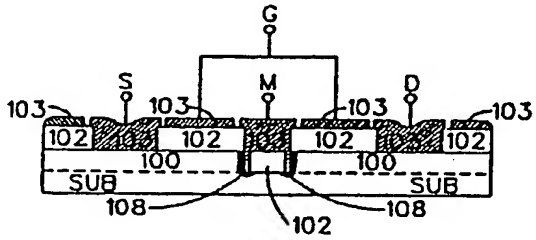

FIG. 11m

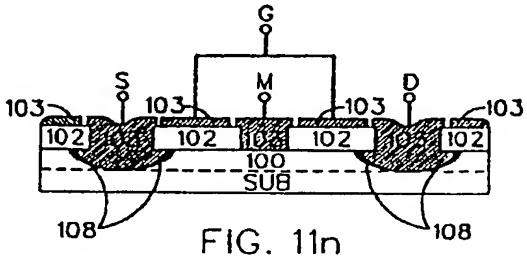

FIG. 11n

Description

[0001] The invention in this Application was developed in part under support provided by a grant from the Energy Related Inventions Program of the United States Federal Department of Energy, under Contract No. DE-FG47-93R701314. The United States Government has certain rights in this invention.

TECHNICAL FIELD

[0002] The present invention relates to Metal Oxide Semiconductor (MOS) device systems and procedures for fabrication thereof. More particularly, the present invention comprises single semiconductor type, Schottky barrier junction inverting and noninverting single devices which demonstrate operational characteristics similar to Complimentary Metal Oxide Semiconductor (CMOS) multiple device systems and which can be used as modulators. The present invention is further a Regeneratively Switching Source Coupled CMOS system of P and N-Channel MOSFETS, which MOSFETS operate only when opposite Polarity Voltages are Applied from the Drain to the Source and from the Gate to the Source thereof, and the Polarity of Voltage applied to the Gate is appropriate to Invert a Channel Region thereof. The present invention is further a Schottky barrier junction voltage controlled switch which demonstrates operational characteristics similar to a nonlatching silicon controlled rectifier. In addition the present invention is, colaterally, an insulator effected, channel end located, minimized Schottky barrier junction area, low leakage current Schottky barrier rectifying junction geometry in etched Intrinsic, N and/or P-Type semiconductor.

BACKGROUND

[0003] The use of N and P-Channel Metal Oxide Semiconductor Field Effect Transistors, (hereinafter MOSFETS), in functional combination to form Complementary Metal Oxide Semiconductor, (hereinafter CMOS), field effect transistor device systems is well known, as are the benefits associated with the use thereof. Said benefits include enabling realization of very low power consumption digital switching logic circuitry such as is found in electronic wrist watches which run for years on one small battery.

[0004] Briefly, a conventional MOSFET is comprised of N or P-type semiconductor substrate in which are formed regions of oppositely doped material, separated by a distance therebetween. The regions of oppositely doped material are termed the "Source" and "Drain" and the distance therebetween is termed the "Channel Region". Diffused rectifying junctions are conventionally formed at the ends of the channel region, both at the source and at the drain. Continuing, atop the channel region surface is present an insulating material, such as silicon dioxide, atop of which insulating material is present a "gate" which is made from an electrically conductive material. Application of a voltage from the Drain-to-Source of a proper polarity, simultaneous with the application of a Gate-to-Source voltage of a proper polarity causes the channel region to "invert" and become of a doping type similar to that in the source and drain regions, thereby providing a conductive pathway between said drain and source. That is, application of a gate-to-source voltage modulates the conductivity of, hence flow of current between, the drain and source. Because the resistivity of the insulating material is high, very little gate current is required to effect modulation of said drain to source current flow. As mentioned above, CMOS device systems comprise a series of electrically connected N and P-channel MOSFET devices, formed on P and N-Type semiconductor respectively. To form CMOS the drain of an N-Channel MOSFET device is electrically connected to the drain of the a P-channel MOSFET device and the source of the P-channel device is connected to a positive voltage (Vd), while the source of the N-channel MOSFET device is connected to a lower voltage (Vs), typically ground. In use, a relatively low, (approximately the voltage applied to the source of the N-channel MOSFET device), gate voltage applied simultaneously to the gates of said electrically connected devices modulates the P channel device so that it conducts, while having no channel conductivity increasing effect on the N channel device. Similar simultaneous application of a relatively high, (with respect to the voltage applied to the source of the N-channel MOSFET device, eg. approximately Vd), gate voltage affects the N and P channel devices in an opposite manner. That is the N-channel device channel conductivity is effectively increased while the P-channel device channel conductivity is not increased. The result being that varying gate-to-source voltage from relatively low to relatively high causes the voltage present at the electrically connected N and P-channel device drains to vary between that applied to the source of the and P-channel device, (Vd), and that applied to the source of the N-channel device, (typically, but not necessarily, ground potential), respectively. As mentioned above, CMOS switching is effected with very little gate current flow, as the insulating material between the gate and the semiconductor is of a very high resistance, (eg. ten-to-the-forteenth ohms). As well, drain to source current flows only briefly at the switching point when both devices are momentarily conducting. This is because current cannot flow through an electrically connected series of MOSFETS when either thereof does not have a conducting inverted channel present. Conventional MOSFET and CMOS operational characteristics are described in numerous circuit design texts such as "Basic Integrated Circuit Engineering" by Hamilton and Howard, McGraw-Hill, 1975.

[0005] While conventional CMOS device systems provide benefits, fabrication thereof is by diffused junction technology which requires many steps, including many photoresist procedures, sequential mask alignments, and various etches. It is to be appreciated that each such step involves an efficiency factor, and thereby introduces defects leading to decreased yield of working devices on a fabrication substrate. In some instances the ratio of working to the total devices attempted on a substrate can be fifty (50%) percent or even less. For instance if a procedure step carries a ninety (90%) percent efficiency factor, (an extremely low value used for demonstrative purposes), after two such steps only eighty-one (81%) percent of the devices will be operational. After six (6) such steps, it should be appreciated, the effective yield of working devices will be less than fifty (50%) percent. Obviously, if the number of steps in a fabrication procedure can be reduced the yield of working devices can be increased. However, conventional diffused junction technology does not allow reducing the number of steps involved in a fabrication procedure below a relatively large number.

[0006] A fabrication procedure which requires a reduced number of fabrication procedure steps to provide functionally equivalent CMOS device systems would therefore be of utility.

[0007] With that in mind it is to be appreciated that an alternative to conventional diffused junction technology is that of Schottky barrier junction technology. The present invention utilizes said Schottky barrier junction technology in a fabrication procedure requiring a relatively few number of steps to provide CMOS device systems. Another benefit of utilizing Schottky barrier technology is that rectifying junctions formed therefrom are "Hot-Carrier" devices. That is majority carriers, rather than minority carriers form the basis of operation. It is well known that Hot Carrier devices react, (ie. switch), faster than do, for instance Diffused Junction based devices. This is because minority carriers need not be withdrawn from a depletion region in a rectifying junction for instance, to proceed from a conducting forward biased state to a nonconducting reverse biased state. Devices formed from Schottky barrier technology therefore can provide inherently faster operation. This point is well documented in an article by Yu, titled "The Metal-Semiconductor Contact: an Old Device with a New Future", IEEE Spectrum, Vol. 7, No. 3, March 1970. As well, it is well known that circuits which utilize "Regenerative switching" provide inherently faster operation. A CMOS system which provides Regenerative Switching and which is fabricated from Hot Carrier Schottky barriers at the Source and Drains of the N and P-Channel MOSFETS which comprise said CMOS System, would therefore provide great utility. No known reference reports, or remotely hints that such a Regeneratively switching CMOS inverter system can be realized, emphasis added. To the Inventor's knowledge, only the present Disclosure teaches N and P-Channel MOSFETS which operate as do those of the present invention. In addition, no known reference suggests that a single device with operational characteristics similar to multiple device CMOS systems is possible.

[0008] A Search of relevant references has provided an article by Hogeboom and Cobbold, titled "Etched Schottky Barrier MOSFETS Using A Single Mask". Said article describes the fabrication of a P-Channel MOSFET on N-type silicon with aluminum forming the rectifying junction Schottky barrier source and drain junctions. (Note that aluminum does not form a rectifying junction Schottky barrier on P-type silicon hence is not an appropriate metal for use in realization of N-channel Schottky barrier MOSFETS). Said article also describes both N and P-Channel conventional diffused junction MOSFETS fabricated using a single mask, but which required a diffusion of a dopant, hence, did not operate based upon Schottky barrier junction presence. Aluminum present provided ohmic contact to diffused regions as in conventional MOSFETS. This paper also suggests the use of vanadium to form source and drain regions. It is also noted that this paper describes use of a silicon dioxide undercutting etch which facilitates self delineation of fabricated devices. (The silicon etchant taught is a mixture of fifty (50) parts acetic acid, thirty (30) parts nitric acid, twenty (20) parts hydrofluoric acid and one (1) part aniline). A Patent to Welch, No. 4,696,093 describes a procedure for fabricating Schottky barrier MOSFETS, including an approach requiring only one-mask and one-etch and the use of chromium, (which after application to silicon is subjected to an annealing procedure to form chromium disilicide), as the metal used to form rectifying source and drain Schottky barrier junctions. A Masters Thesis presented by James D. Welch at the University of Toronto in 1974 titled "Design and Fabrication of Sub-Micron Channel MOS Transistors by Double Ion-Implantation" mentions Schottky barrier rectifying junctions discovered to exist after a thirty (30) minute, six-hundred-fifty (650) degree centigrade anneal of chromium present on the back, unpolished, side of an N-type silicon substrate. The reverse breakdown voltage of said rectifying junctions was found to be upwards of eighty (80) volts. However, said thesis work did not include investigation of annealing deposited chromium on P-type silicon. A paper by Lebedev and Sultanov, in Soviet Physics Semiconductors, Vol. 4, No. 11, May 1971, pages 1900-1902 teaches the chromium diffused into P-type Silicon at high, (eg. twelve hundred (1200) degrees centigrade), for long periods of time, (eg. twenty (20) to fifty (50) hours), dopes said P-type silicon N-type. Nothing, however, is stated regarding the properties of chromium disilicide formed by annealing a thin film of chromium which has been deposited upon said P-type silicon silicon at lower temperatures. A paper by Olowolafe et al., J. App. Physics, Vol 47, No. 12, Dec. 1976 describes investigation of the formation of Chromium Disilicide by annealing deposited chromium to silicon. A Patent to Koeneke et al, No. 4,485,550 describes a Schottky barrier MOSFET fabricated using Platinum as the Schottky barrier forming metal in Source and Drains regions thereof. Said Patent reports that the Schottky barrier MOSFETS reported can one for one replaced diffused junction MOSFETS in a CMOS system to provide a Latch-up proof result. A paper by Lepselter and Sze, titled "SB-IGFET: An Insulated-Gate Field Effect Transistor Using Schottky Barrier Contacts for Source and Drain",

in the Proceedings of the IEEE, August 1968, pages 1400 through 1402 describes a similar P-Channel Schottky barrier insulated gate field effect transistor, (ie. IGFET), fabricated using Schottky barrier contacts for source and drain. Said IGFET again utilized platinum silicide in the formation of the source and drain junctions. It is stated that during operation the source junction of the device is reverse biased in the inverted channel region and that reverse leakage or tunneling current therethrough is what applied gate voltage modulates. The Lepselter et al. article however, makes no mention of the use of Schottky barriers to form N-Channel devices on P-type silicon, and reports operational characteristics are achieved therefrom which are consistent with diffused junction MOSFETS. In fact, owing to the rather large reverse barrier height difference between platinum silicide and N-type silicon, (ie. 0.85ev), and between platinum silicide and P-type silicon, (ie. 0.25ev), it is unlikely that N-channel devices would be operable, or even if they were, that an effective CMOS device system could be achieved using platinum-silicide to form both N and P-channel devices. This is because the MOSFET devices in a CMOS device system must have essentially symetrical and Complementary operational characteristics to provide efficient switching capability. However, as disclosed in the Detailed Description Section of this Disclosure, platinum might be very well suited for forming a single device equivalent to CMOS on N-type silicon. The Lepselter et al. article provides an equation for calculating tunneling current density through a reverse biased Schottky barrier junction:

$$J = \exp\left(\frac{-4}{3} \frac{(\mathrm{SQRT}\ 2m^*(PHI)^{\frac{3}{2}})}{(3\ q\ h\ E)} \right)$$

where E is the electric field induced by application of a

voltage across the junction,
m* is the effective mass,
h is Boltzman's constant,
PHI is the reverse barrier potential, and
J is current density.

The Lepselter et al. article is incorporated by reference herein. Many texts describe Schottky barrier junctions and they will not be further discussed in this Disclosure.

[0009] A Patent to Lepselter, No. 4,300,152 describes a (CMOS) device in which at least one of the N and P-Channel devices is a Schottky barrier based device. It is taught that a (CMOS) device system utilizing such is immune to latch-up based upon Silicon Controlled Rectifier-like action in (CMOS) device systems.

[0010] A Patent to Mihara et al., No. 5,049,953 describes a Schottky barrier device in which a shield layer of a second conductivity type imposed between a Schottky barrier and a substrate serves to reduce leakage current.

[0011] Continuing, a recent Patent to Honma et al., No. 5,177,568 describes a tunnel injection type semiconductor device having a Metal-Insulator-Silicon (MIS) structure comprising a semiconductor region, a source, a drain and a gate electrode wherein said source and drain are composed of a metal or metal compound member, respectively, and wherein both have an overlapping portion with said gate electrode. The Source provides a Schottky barrier junction to said semiconductor region while said drain provides an non-rectifying contact to said semiconductor region. A tunneling current is caused to flow across a Schottky barrier junction between said source and said drain, controlled by a gate voltage. This Patent describes formation of a (CMOS) device system wherein schottky barriers serve as source region contacts to N and P-type silicon and wherein interconnected drain contacts are non-rectifying. The devices described in this Patent are very interesting, but fabrication thereof obviously requires rather complicated channel region doping profile effecting and yield reducing steps to effect rectifying junctions at the source and non-rectifying junctions at the drain of a (MOSFET) structure. That is, economic savings as compared to conventional diffused junction (MOSFET) fabrication would seem to be reduced by the channel doping requirements. Use of doping and varying band gap materials are disclosed as approaches to realizing the devices described. It is also noted that the devices described apparently operate, (show gate controlled drain current flow), with the semiconductor between source and drain "accumulated" while a source Schottky barrier junction is reverse biased by applied drain to source voltage polarity. That is for a N-type substrate, a positive gate to source voltage is applied and for a P-type semiconductor a negative polarity gate to source voltage would be applied. As will be seen in following Sections herein, present invention devices preferably operate by effecting "inversion" in semiconductor between source and drain. For instance, for an N-type sem-

iconductor the applied gate voltage during operation is negative in polarity when applied drain to source voltage is positive in polarity. For P-type semiconductor the applied gate to source voltage polarity during operation is positive while the drain to source voltage polarity is negative. This is cited as a major distinction in operational bases between the Honma et al. devices and the present invention devices.

[0012] No known reference teaches, as does the present invention disclosure, that a relatively simple fabrication procedure utilizing both N and P-type semiconductor can simultaneously efficiently form low, insulator effected, leakage current balanced Schottky barrier rectifying junctions in (MOSFET) Source and Drain regions on both said N and P-type semiconductor, preferably in a single semiconductor substrate, thereby allowing essentially balanced complimentary N and P-channel (MOSFETS) with Schottky barrier junctions at both source and drain to be easily achieved, particularly on a single substrate. This is a very significant point as it would not be obvious to one skilled in the art that such a single simultaneous procedure should exist or what elements, (eg. metal, metal-silicide and semiconductor), should be utilized in said procedure or what the procedure should be followed. The present invention provides missing teachings along with documented experimental results supporting said teachings. The present invention, however, goes even further and teaches that a single device equivalent to (CMOS) can be achieved on a single dopant type, or even intrinsic, semiconductor substrate utilizing Schottky barrier technology, with or without leakage current reducing insulator material presence, by provision of a voltage monitoring contact to the channel region under the gate electrode of a Schottky barrier (MOSFET) structure. As described elsewhere in this disclosure, said device operates because Schottky barriers formed using appropriate semiconductors and metals and/or metal silicides form rectifying junctions with either N or P-type semiconductor, and effective (MOSFET) channel region semiconductor doping can be effected by application of a gate voltage in a (MOSFET) structure. All known (CMOS) devices require the presence of N and P-type doped semiconductor. The present invention teaches that a single device equivalent to (CMOS), in contrast, requires only a single type, (N or P-type), semiconductor substrate be present, emphasis added. This enables cost savings and improved fabrication efficiency.

[0013] No known reference states that a CMOS device system which provides regenerative switching characteristics should be fabricated wherein Schottky barriers serve as source and drain rectifying junctions in both N and P-Channel MOSFETS in either separate semiconductor substrates, or preferably on a single semiconductor substrate, where said N and P-Channel MOSFETS provide Operational Drain Schottky barrier junction Current vs. Applied Drain Schottky barrier to Source Schottky barrier junction Voltage, as a function of Applied Gate Voltage, both said Applied Voltages being referenced to said Source Schottky barrier junction as a common terminal, only wherein said Applied Drain Schottky barrier junction to Source Schottky barrier junction Voltage, and Applied Gate Voltage are of opposite polarity. In addition no known reference documents that the a single fabrication procedure utilizing both N and P-type semiconductor can simultaneously efficiently form sufficiently balanced Schottky barrier rectifying junctions on both said N and P-type semiconductor, preferably in a single semiconductor substrate, thereby allowing essentially balanced Complementary N and P-channel MOSFETS to be easily achieved, particularly on a single substrate, by a common simultaneous fabrication procedure. In addition, as mentioned above, no known reference even remotely hints that a CMOS system can be fabricated which demonstrates regenerative switching characteristics in use. This is a very significant point as without some insight as to the fact that such a regenerative switching CMOS system can be achieved, it would not be obvious to one skilled in the art to even attempt to fabricate such a regeneratively switching CMOS System, or what elements, (eg. metal, metal-silicide and semiconductor), might be utilized etc. in an attempt to do such. The present invention provides missing teachings along with documented experimental results supporting said teachings.

[0014] While the above shows that it is known to form MOSFETS using Schottky barriers at Source and Drain, and that the use of Chromium in the formation of Schottky barrier junctions is known, no known reference remotely hints that the use of Chromium at Source and Drain in the fabrication of Schottky barrier MOSFETS should provide Schottky barrier MOSFETS which operate as do present invention Schottky barrier MOSFETS. Further, no known reference suggests that a CMOS System can be achieved in which the Sources are electrically interconnected, (rather than Drains as in conventional Diffused Junction and reported Schottky barrier MOSFETS), which CMOS System demonstrates Regenerative Hot Carrier Based, (hence, speed enhanced), Switching in use, emphasis added.

[0015] Two Patents to Proebsting, Nos. 4,985,643 and 5,343,090 are also identified as they serve to document that speed enhancement in CMOS circuits is desirable. Said invention utilizes feedback between stages in a circuit to allow use of substantially all of a signal to turn on devices, rather than require that a portion thereof be utilized to turn devices off.

[0016] It is mentioned that in a proprietory report, dated January 10, 1991, which was prepared by the National Institute of Standards and Technology, (NIST) in support of the grant which has funded the work disclosed herein, it was concluded that the present invention could have an impact on energy conservation and utilization and that if the projected performance of the invention can be achieved, then commercial success seems assured. Said proprietory NIST report was provided in response to a confidential application for grant funds submitted to the funding agency years earlier by the inventor herein, in search of support to allow actual present invention reduction to practice.

[0017] Finally, it is emphasized that teachings obviating the present invention are found only in this Disclosure,

emphasis added. Without the present Disclosure a researcher would not find any suggestion that a CMOS System with Regenerative Hot Carrier Based Switching Characteristics should be realizable, or that single devices with characteristics similar to CMOS should be realizable.

[0018] The present invention teaches an experimentally verified MOSFET system and a recommended fabrication procedure therefore.

DISCLOSURE OF THE INVENTION

[0019] The present invention is based in the use of Schottky barrier junctions, formed from non-semiconductor and semiconductor components, which Schottky barrier junctions have as a non-semiconductor component a material which forms a rectifying junction with either N or P-type semiconductor, whether said semiconductor doping type is metalurigically or field induced. Said present invention includes:

a. Inverting and non-inverting single devices which inverting and non-inverting single devices operate similar to conventional multiple device CMOS systems, and which can be operated as modulators;

b. N and P-Channel Schottky barrier MOSFETS which operate only when a Gate voltage of an appropriate polarity to invert a semiconductor type is applied simultaneously with application of an opposite polarity voltage to the Drain thereof, both said voltages being with respect to the Source thereof;

c. Regeneratively switching multiple device Schottky barrier MOSFET CMOS systems;

d. Schottky barrier based devices which demonstrate operating characteristics similar to a "non-latching" conventional silicon controlled rectifier SCR; and

e. A Schottky barrier junction area limiting, etched semiconductor well, and insulator effected geometry.

[0020] The most important embodiment of the present invention is an inverting single Metal Oxide Semiconductor (MOS) device with operating characteristics similar to multiple device Complimentary Metal Oxide Semiconductor (CMOS) systems, which can be used as a modulator, wherein an applied gate voltage controls a voltage present at an essentially electrically isolated terminal thereof. Said most important embodiment comprises first and second essentially non-rectifying channel region junctions in a surface region of a single doping type semiconductor selected from the group consisting of N-type, P-type, Intrinsic, N-type and Intrinsic, P-type and Intrinsic, N-type on insulator, and P-type on insulator. Said first and second essentially non-rectifying channel region junctions are separated by first and second semiconductor channel regions from electrically interconnected rectifying Schottky barrier to channel region junctions, wherein first and second gates to which semiconductor channel region doping type effecting modulating gate voltage can be applied are associated with said first and second semiconductor channel regions. Said first and second gates are offset from said first and second semiconductor channel regions, respectively, by insulating material, such that application of a sufficient negative voltage to the first and second gates will attract holes into said first and second semiconductor channel regions, and such that application of a sufficient positive voltage to the first and second gates will attract electrons into said first and second semiconductor channel regions. The purpose of applying such gate voltage is to modulate the effective doping type of said first and second semiconductor channel regions, such that when a constant polarity voltage is applied between said first and second essentially non-rectifying channel region junctions one rectifying Schottky barrier to channel region junction forward conducts while the other simultaneously does not, which Schottky barrier to channel region junction forward conducts at a specific time being determined by semiconductor doping type in said first and second semiconductor channel regions, said semiconductor doping type being determined by applied gate voltage polarity. The essentially electrically isolated terminal electrically contacts, via a junction thereto, said electrically interconnected rectifying Schottky barrier to channel region junctions between said first and second semiconductor channel regions and during use monitors a constant polarity voltage applied to one of the first and second essentially non-rectifying channel region junctions, which constant polarity voltage appears at said essentially electrically isolated terminal essentially through the forward conducting Schottky barrier to channel region junction. Said constant polarity voltage monitored by said essentially electrically isolated terminal decreases when the gate voltage applied to said first and second gates is increased. The basis of operation being that said Schottky barrier junctions are formed between said first and second semiconductor channel regions and a material which provides a rectifying junction to a semiconductor channel region when it is doped either N or P-type. Said preferred embodiment can be include at least one of said Schottky barrier to channel region junctions being formed in a region etched into said semiconductor, said etched semiconductor being partially comprised of insulating material, the purpose thereof being to reduce leakage current by limiting the area of Schottky barrier to channel region junctions in contact with said semi-

conductor to regions at ends of said semiconductor channel regions. Said inverting single Metal Oxide Semiconductor (MOS) device with operating characteristics similar to multiple device Complimentary Metal Oxide Semiconductor (CMOS) systems can be fabricated from silicon where the Schottky barrier to channel region junctions are formed between said silicon and at least one material selected from the group consisting of chromium, molybdenum, tungsten, vanadium, titanium, platinum and a silicide of any thereof.

[0021] An important variation of the present invention preferred embodiment is a non-inverting single Metal Oxide Semiconductor (MOS) device with operating characteristics similar to multiple device Complimentary Metal Oxide Semiconductor (CMOS) systems and which can be used as a modulator, in which an applied gate voltage controls a voltage present at an essentially electrically isolated terminal thereof. Said important variation can comprise a geometry which presents with a single channel region or with multiple channel regions.

[0022] In the case where a single channel region is present, said embodiment comprises a semiconductor channel region and two rectifying Schottky barrier to channel region junctions in a surface region of a single doping type semiconductor, selected from the group consisting of N-type, P-type, Intrinsic, N-type and Intrinsic, P-type and Intrinsic, N-type on insulator, and P-type on insulator. Said rectifying Schottky barrier to channel region junctions are separated by said semiconductor channel region, and a gate to which semiconductor channel region doping type modulating voltage can be applied is associated with said semiconductor channel region. Said gate is offset from said semiconductor channel region by an insulating material, such that application of a sufficient negative voltage to the gate will attract holes into said semiconductor channel region, and such that application of a sufficient positive voltage to the gate will attract electrons into said semiconductor channel region, the purpose of applying such gate voltage being to modulate the effective doping type of said semiconductor channel region. When when a constant polarity voltage is applied between said rectifying Schottky barrier to channel region junctions one thereof forward conducts to the channel region while the other thereof simultaneously does not, which Schottky barrier to channel region junction forward conducts at a specific time being determined by semiconductor doping type in said semiconductor channel region, said semiconductor doping type being determined by applied gate voltage polarity. The essentially electrically isolated terminal electrically contacts, via a junction thereto, said channel region and during use monitors a constant polarity voltage applied to one of the rectifying Schottky barrier to channel region junctions, which constant polarity voltage appears at said essentially electrically isolated terminal essentially through the forward conducting Schottky barrier to channel region junction, which constant polarity voltage monitored by said essentially electrically isolated terminal increases when the voltage applied to said gate is increased. The basis of operation is that said Schottky barrier junctions are formed between said semiconductor channel region and a material which provides a rectifying junction to said semiconductor channel region when it is doped either N or P-type.

[0023] In the case where more than one channel region is present, said embodiment comprises first and second rectifying channel region junctions in a surface region of a single doping type semiconductor selected from the group consisting of N-type, P-type, Intrinsic, N-type and Intrinsic, P-type and Intrinsic, N-type on insulator, and P-type on insulator. Said first and second rectifying channel region junctions are separated by first and second semiconductor channel regions from electrically interconnected essentially non-rectifying channel region junctions, wherein first and second gates to which semiconductor channel region doping type effecting modulating gate voltage can be applied are associated with said first and second semiconductor channel regions. Said first and second gates are offset from said first and second semiconductor channel regions, respectively, by insulating material, such that application of a sufficient negative voltage to the first and second gates will attract holes into said first and second semiconductor channel regions, and such that application of a sufficient positive voltage to the first and second gates will attract electrons into said first and second semiconductor channel regions. The purpose of applying such gate voltage is to modulate the effective doping type of said first and second semiconductor channel regions, such that when a constant polarity voltage is applied between said first and second rectifying channel region junctions one rectifying Schottky barrier to channel region junction forward conducts while the other simultaneously does not. Which Schottky barrier to channel region junction forward conducts at a specific time is determined by semiconductor doping type in said first and second semiconductor channel regions, said semiconductor doping type being determined by applied gate voltage polarity. Said essentially electrically isolated terminal electrically contacts, via a junction thereto, said electrically interconnected essentially non-rectifying channel region junctions between said first and second semiconductor channel regions and during use monitors a constant polarity voltage applied to one of the first and second rectifying channel region junctions. Said constant polarity voltage which appears at said essentially electrically isolated terminal is essentially through the forward conducting Schottky barrier to channel region junction, and said constant polarity voltage monitored by said essentially electrically isolated terminal decreases when the gate voltage applied to said first and second gates is decreased. Again, the basis of operation is that said Schottky barrier junctions are formed between said first and second semiconductor channel regions and a material which provides a rectifying junction to a semiconductor channel region when it is doped either N or P-type.

[0024] Said non-inverting single Metal Oxide Semiconductor (MOS) devices with operating characteristics similar to multiple device Complimentary Metal Oxide Semiconductor (CMOS) systems can be fabricated from silicon where the

Schottky barrier to channel region junctions are formed between said silicon and at least one material selected from the group consisting of chromium, molybdenum, tungsten, vanadium, titanium, platinum and a silicide of any thereof.

[0025] A method of configuring an Metal Oxide Semiconductor (MOS) device with operating characteristics similar to Complimentary Metal Oxide Semiconductor (CMOS) systems and which can be used as a modulator, can comprise the steps of:

a. providing two Metal Oxide Semiconductor Field Effect Transistor (MOSFET) devices, each formed in a surface region of the same single doping type semiconductor selected from the group consisting of N-type, P-type, Intrinsic, N-type and Intrinsic, P-type and Intrinsic, N-type on Insulator, and P-type on Insulator, one said (MOSFET) device comprising two junctions, termed source and drain, separated by a first semiconductor channel region, and the second (MOSFET) device comprising two junctions, termed source and drain, separated by a second semiconductor channel region, wherein gates to which semiconductor channel region inverting voltage can be applied are associated with each of the first and second semiconductor channel regions are offset from said first and second semiconductor channel regions by insulating material, such that during use application a sufficient positive voltage to said gates will attract electrons to said first and second semiconductor channel regions, and such that application of sufficient negative voltage to said gates will cause attraction of holes to both of said first and second semiconductor channel regions, the purpose of applying such gate voltage being to, modulate the effective doping type of said first and second semiconductor channel regions between respective source and drain junctions, which source junctions are each essentially non-rectifying, and which drain junctions are rectifying Schottky barrier junctions, said rectifying Schottky barrier and essentially non-rectifying junctions each comprising a semiconductor and non-semiconductor component;

b. electrically interconnecting a non-semiconductor component of a member of the group consisting of: (the rectifying Schottky barrier drain junction associated with said first semiconductor channel region and the essentially non-rectifying source junction associated with said first semiconductor channel region), and, respectively, a member of the group consisting of: (the rectifying Schottky barrier drain junction associated with said second semiconductor channel region and the essentially non-rectifying source junction associated with said second semiconductor channel region);

c. electrically interconnecting said gates, such that during operation electrically noninterconncted junctions are held at different voltages, and application of a gate voltage controls effective semiconductor channel region doping type in both (MOSFET) devices, and thus which rectifying Schottky barrier drain junction forward conducts and which does not forward conduct, thereby controlling the voltage present at the nonsemiconductor components of the electrically interconnected junctions essentially through said forward conducting rectifying semiconductor Schottky barrier drain junction;
the basis of operation being that said Schottky barrier junctions are formed between said first and second semiconductor channel regions and a material which provides a rectifying junction to a semiconductor channel region when it is doped either N or P-type.

[0026] The present invention also recognizes that Schottky barrier reverse bias leakage per unit area of junction, is greater than that associated with diffused junction. Hence the present invention provides for formation of Schottky barrier junction(s) in region(s) etched into said semiconductor, which etched region(s) are partially comprised of insulating material, the purpose thereof being to reduce leakage current by limiting the area of Schottky barrier junction in contact with said semiconductor to a region near an end of said semiconductor channel region.

[0027] Where a Schottky barrier Metal Oxide Semiconductor (MOS) device is fabricated, said etched region in said semiconductor is such that the insulating material by which the gate is offset from the semiconductor channel region is undercut, and such that said Schottky barrier junction is present only at the end of said semiconductor channel region which is located under said gate offsetting insulator material.

[0028] It was a discovery in research leading to the present invention that Schottky barrier MOSFETS formed using Chromium as a Schottky barrier formeing material demonstrated unique operating characteristics. Said Schottky barrier MOSFETS demonstrate Drain current flow only where an applied Gate voltage is appropriate to invert the semiconductor involved, and where the Drain voltage is of an opposite polarity thereto. When a P and N-channel Schottky barrier MOSFET fabricated utilizing chromium as the Schottky barrier forming material it is a consequence that A Complementary Metal Oxide Semiconductor (CMOS) System formed therefrom demonstrates regenerative switching in use. Such a regenerative switching (CMOS) system comprises an N-Channel Schottky barrier Metal Oxide Semiconductor Field Effect Transistor (MOSFET) in series combination with a P-Channel Schottky barrier MOSFET. The P-Channel Schottky barrier MOSFET comprises a device formed in a surface region of an N-type Semiconductor, said P-Channel MOSFET comprising two Schottky barrier junctions, termed Source and Drain Schottky barrier junctions,

which Source and Drain Schottky barrier junctions are separated by an N-type Semiconductor Channel region, in which P-Channel Schottky barrier MOSFET a Gate is offset from said N-type Semiconductor Channel Region by a first region of insulator material. Said P-Channel Schottky barrier MOSFET provides significant Drain Schottky barrier junction Current vs. Applied Drain Schottky barrier junction to Source Schottky barrier junction Voltage as a function of Applied Gate Voltage Operating Curves only when the Voltage applied to the Drain Schottky barrier junction is of a Positive Polarity, and when the Voltage applied to the Gate is of a Negative Polarity so as to induce an inverted P-type Channel Region, both said Drain Schottky barrier junction and Gate Voltages being referenced to the Source Schottky barrier junction as a common terminal. The N-Channel Schottky barrier MOSFET comprises a device formed in a surface region of a P-type Semiconductor, said N-Channel MOSFET comprising two Schottky barrier junctions, termed Source and Drain Schottky barrier junctions, which Source and Drain Schottky barrier junctions are separated by a P-type Semiconductor Channel region, in which N-Channel Schottky barrier MOSFET a Gate is offset from said P-type Semiconductor Channel Region by a second region of insulator material, which N-Channel Schottky barrier MOSFET provides significant Drain Schottky barrier junction Current vs. Applied Drain Schottky barrier junction to Source Schottky barrier junction Voltage as a function of Applied Gate Voltage Operating Curves only when the Voltage applied to the Drain Schottky barrier junction is of a Negative Polarity, and when the Voltage applied to the Gate is of a Positive Polarity so as to induce an inverted N-type Channel Region, both said Applied Drain Schottky barrier junction and Gate Voltages being referenced to the Source Schottky barrier Junction as a common terminal. When the Source Schottky barrier junction of said N-Channel Schottky barrier MOSFET and the Source Schottky barrier junction of said P-Channel Schottky barrier MOSFET are electrically interconnected to one another, and said Gates of said N and P-Channel Schottky Barrier MOSFETS are electrically interconnected to one another, and when a Positive Polarity Voltage is applied to the electrically noninterconnected Drain Schottky barrier junction of the P-Channel Schottky barrier MOSFET, (said Positive Polarity being with respect to the Voltage applied to the electrically noninterconnected Drain Schottky barrier junction of the N-Channel Schottky barrier MOSFET), and Voltage at the electrically interconnected Gates is set to essentially that applied to the electrically noninterconnected Drain Schottky barrier junction of the N-channel Schottky barrier MOSFET, then the voltage at the electrically interconnected Source Schottky barrier junctions of the N and P-Channel Schottky barrier MOSFETS regeneratively switches to essentially that applied to the electrically noninterconnected Drain Schottky barrier junction of the P-Channel Schottky barrier MOSFET. And when the Voltage at the electrically interconnected Gates is set to essentially that applied to the electrically noninterconnected Drain Schottky barrier junction of the P-Channel Schottky barrier MOSFET, the voltage at the electrically interconnected Source Schottky barrier junctions regeneratively switches to essentially that applied to the electrically noninterconnected Drain Schottky barrier junction of the N-Channel Schottky barrier MOSFET. It is specifically noted that a suitable Semiconductor for practicing the present invention is Silicon, and that Source and Drain Schottky barrier junctions in both the N and P-Channel MOSFETS can be formed between said Silicon and at least one member of the group consisting of Chromium and Chromium Disilicide.

[0029] (Note, it is to be understood in the foregoing that Schottky barrier junctions are comprised of two components, a semiconductor component and a non-semiconductor component. Applied Drain and Source Schottky barrier voltages are applied to non-semiconductor components, and Drain Schottky barrier current is measued by contacting a non-semiconductor component of a Schottky barrier junction).

[0030] It is another result of the present invention that a method of configuring a Metal Oxide Semiconductor (MOS) gate voltage controlled rectification direction device and voltage controlled switch with operating characteristics similar to a non-latching Silicon Controlled Rectifier (SCR) can comprise:

a. providing a (MOSFET) with a rectifying Schottky barrier first junction and a non-rectifying second junction in a surface region of a semiconductor, said first and second junctions being separated by a channel region in said semiconductor, said channel region having an insulator region and gate sequentially situated adjacent thereto;

b. applying a constant voltage between said second and first junctions of a polarity such that said rectifying Schottky barrier first junction is reverse biased, but conducts forward biased current if said second to first junction voltage polarity is reversed;

c. applying a gate voltage such that the channel region is caused to be inverted by the attraction of electrons thereto, thereby effecting a forward bias between said inverted channel region and said rectifying Schottky barrier first junction, such that forward biased current flows therethrough;

the basis of operation being that said Schottky barrier first junction is formed between said semiconductor channel region and a material which provides a rectifying junction to said semiconductor channel region when it is doped either N or P-type.

[0031] The present invention will be better understood by reference to the Detailed Disclosure Section, in coordination

with the Drawings.

SUMMARY OF THE INVENTION

[0032] It is therefore a primary purpose of the present invention to teach the use of single doping type and/or intrinsic silicon in reailzation of single device inverting and single device non-inverting systems, fabricated on a single type semiconductor, which single inverting and non-inverting devices, and variations thereof, demonstrate characteristics similar to multiple device (CMOS) systems and can be operated as modulators, nonlatching (SCR's) and/or gate voltage controlled direction of rectification devices.

[0033] It is another primary purpose of the present invention to teach a CMOS device system comprising two metal-N-type and/or metal-silicide-N-type semiconductor rectifying junctions separated by a first channel region, in functional combination with two metal-P-type and/or metal-silicide-P-type semiconductor rectifying junctions separated by a second channel region, said first and second channel regions having first and second gates offset thereform by first and second regions of insulating material, which CMOS device system demonstrates regenerative switching in use.

[0034] It is a still yet another purpose of the present invention to teach a suitable device self-delineating fabrication procedure for MOSFET device systems utilizing Schottky barriers, which fabrication procedure can simultaneously allow fabrication of both N and P-Channel MOSFETS, and requires a lessor number of defect introducing fabrication steps as compared to fabrication schemes utilizing diffused junction technology.

[0035] It is yet another purpose of the present invention to teach a low leakage current Schottky barrier (MOSFET) device structure which provides Schottky barrier junctions only at the ends of a semiconductor channel region, and a fabrication procedure for realization thereof.

[0036] It is a further purpose of the present invention to disclose experimentally obtained results which demonstrate operational characteristics of Schottky barrier technology derived MOSFET devices fabricated by the disclosed fabrication procedure in which chromium was used as a Schottky barrier forming metal.

BRIEF DESCRIPTION OF THE DRAWINGS

[0037]

Fig. 1(a) shows a top view of a conventional (MOSFET).

Fig. 1(b) shows a side cross-sectional view of a conventional (MOSFET) taken at a-a in Fig. 1(a).

Fig. 2(a) shows a top view of a conventional (CMOS) device system.

Fig. 2(b) shows a side cross-sectional view of a conventional (CMOS) device system taken at b-b in Fig. 2(a).

Fig. 3 shows a side cross-sectional view of a Schottky barrier (MOSFET) device system of the present invention.

Fig. 4 shows a side cross-sectional view of a modified Schottky barrier (MOSFET) device system of the present invention.

Fig. 5 demonstrates the formation of a metal-silicide when a metal which has been deposited upon a semiconductor substrate is annealed.

Figs. 6a and 6b show (MOSFET) drain-current vs. drain-to-source voltage curves, as a function of gate-to-source voltage, provided by a device formed on P-type silicon with a 75 micron wide gate, wherein chromium was deposited in drain and source regions and annealed thereto.

Figs. 7a and 7b shows (MOSFET) drain-current vs. drain-to-source voltage curves, as a function of gate-to-source voltage, provided by a device formed on N-type silicon with a 15 mil wide gate, wherein chromium was deposited in drain and source regions and annealed thereto.

Fig. 8a shows (CMOS) curves such as provided by a seriesed combination of (MOSFET) devices, which provide drain-current vs. drain-to-source voltage curves as demonstrated in Figs. 6a, 6b and 7a, 7b, and by single device equivalents to (CMOS) systems.

Fig. 8b shows a circuit symbol for a (CMOS) circuit provided by a seriesed combination of (MOSFET) devices,

which provide drain-current vs. drain-to-source voltage curves as demonstrated in Figs. 6a, 6b and 7a, 7b.

Figs. 9(a) through 9(j) show a silicon substrate at various stages of fabrication of (MOSFET) devices using a preferred fabrication process.

Figs 9(k) through 9(m) show structures similar to those shown in Figs. 3 and 4, but fabricated by the preferred fabrication method demonstrated by Figs. 9(a) through 9(k).

Figs. 10(a) through 10(i) show steps in fabrication of a non-inverting single device equivalent to (CMOS), and Figs. 10(j) through 10(r) show steps in fabrication of an inverting single device equivalent to (CMOS).

Figs. 11(ao) through 11(go), 11(a1) through 11(g1), 11(a2) through 11(g2p), and 11(a3) through 11(g3) show fabrication steps utilized in arriving at a low leakage Schottky barrier junction.

Figs. 11(ha), 11(hb), 11(i), 11(j) and 11(k) show various (MOSFET) geometries incorporating low leakage current Schottky barrier junctions.

Figs. 11(l), 11(m), 11(n) and 11(o) show various geometries for single device equivalents to (CMOS) incorporating low leakage current Schottky barrier junctions.

Figs. 12(a) and 12(b) show circuit symbols for conventional diffused junction P-Channel and N-Channel (MOSFETS).

Figs. 13(a) and 13(b) show circuit symbol representations for conventional diffused junction and for Schottky barrier (MOSFET) (CMOS) systems.

Fig. 14 shows circuit symbols for a balanced pair of Schottky barrier (MOSFETS) such as can be used in operational amplifiers.

Figs. 15(a) and 15(b) show active Schottky barrier (MOSFETS) with (MOSFET) loads. Active devices are shown as N-Channel but P-Channel (MOSFETS) could also be used.

Figs. 16(a) and 16(b) show circuit diagrams for the inverting and non-inverting single device equivalents to (CMOS) shown in Figs. 10i & 11m and Figs. 10q, 10r & 11n respectively.

DETAILED DESCRIPTION

[0038] Turning now to the Drawings, there is shown in Figs. 1a and 1b a conventional diffused junction silicon substrate MOSFET (1). Shown are a silicon substrate (4) of N or P-type doping with oppositely doped diffused source (2) and drain (3) regions present therein. Shown as well are gate (5) and gate pad (5a), with silicon dioxide (16) present between said gate (5) and a channel region thereunder between said source (2) and drain (3). Figs. 2a and 2b show a CMOS device system (10) comprising a substrate with regions of N (11) and P-type (12) doping. Diffused source (2a) and (3b) and diffused drain (3a) and (2b) regions, of opposite type doping with respect to the type of substrate respectively with which they are associated, are shown on each of the N (11) and P-type (12) regions. Also shown are gates (6) and (7) and gate pads (6a) and (7a). During use gates (6) and (7) can be electrically interconnected, and drain (3a) can be electrically interconnected to drain (2b). Source (2a) can be connected to an external positive voltage (Vdd) and source (3b) connected to external voltage (Vss) which is typically ground. When a relatively low gate voltage is simultaneously applied to the electrically interconnected gates (6) and (7) the P-Channel MOSFET on the N-type silicon (11) will have an inverted P-type channel region formed between its source (2a) and drain (3a), hence will provide a reduced resistivity therebetween. The MOSFET on the P-type (12) silicon will have an accumulated channel region and will continue to demonstrate a high resistivity. (Note that as used herein the term "inversion" means that a gate induced electric field causes silicon type to reverse in a channel region and the term "accumulation" means that a gate induced electric field causes a silicon type to become more so said type, (eg. N or P-type) in a channel region). The voltage applied to the source (2a) will therefore appear at the electrical connection between drain (3a) and drain (2b). It should be appreciated that application of a relatively high gate voltage, (eg. approximately Vdd), will cause the voltage applied to the source (3b) to appear at the electrical connection point between drain (3a) and drain (2b). That is, a low resistivity inverted channel will form in the N-channel device formed on the P-type (12) silicon while the P-channel device formed on the N-type (11) silicon will demonstrate accumulated channel high drain (3a) to source (2a) resistivity. As the gate

oxide is of a high resistance, (eg. ten-to-the-forteenth ohms), little gate current is required to switch the identified voltage at the electrical connection between drain (3a) and drain (2b). Also, as one of the devices is nearly always off during operation, except momentarily at the point of switching, very little source (2a) to source (3b) current flows. It should then be appreciated that the CMOS device system is very energy efficient. CMOS devices systems then allow applied gate voltage control of the voltage present at an essentially electrically isolated terminal.

[0039] Turning now to Fig. 3, there is shown a CMOS device system appropriate to the present invention. Both N (11) and P-type (12) doped regions are shown in a silicon substrate. Shown also are silicon dioxide (16), gates (15a) and (15b), sources (2a) and (3b) and drains (2b) and (3a) with metal (15) present, said metal (15) being discontinuous between that atop the silicon dioxide (16) and atop the N-type (11) and P-type (12) silicon. The gates (15a) and (15b) are shown electrically interconnected as are drain (2b) and drain (3a). Fig. 5 demonstrates that an anneal of metal (15) in contact with silicon can cause formation of a silicide (15s) at the metal-silicon interface or otherwise effects a Schottky barrier rectifying junction, between said metal (15) and said silicon. This is the case whether the silicon is N (11) or P-type (12), when for instance, the metal is chromium or molybdinum. Fig. 5 demonstrates that a Schottky barrier is comprised of semiconductor (15s) and nonsemiconductor (15) components. Also, though not explicitly shown it is to be understood that said silicide can form laterally, into a channel region under a gate (15a) (15b), as well as vertically into a semiconductor substrate.

[0040] It should be appreciated that deposition of metal (15) upon a substrate etched as demonstrated in Fig. 3 can provide a self delineated CMOS device system if the metal deposited is not too thick and deposited by a line-of-sight technique, and it forms a silicide with silicon when annealed thereto. Fig. 4 shows a variation in which the oxide is removed between drain (2b) and drain (3a) providing immediate electrical interconnection therebetween.

[0041] The drain-current vs. drain-to-source-voltage operational curves of N-Channel and P-Channel, respectively, devices as shown in Figs. 3 and 4 are similar to those of normal MOSFETS, with the exception that drain current flows in a direction opposite to that in conventional MOSFETS. (Note that the parameter analyzer provides output data indicating the drain voltage as negative or positive with respect to the source, which is held at ground potential. However, as the tested Schottky Barrier MOSFETS are geometrically symetrical with regard to the drain and source relation to the gate, (see Figs. 1-4 to appreciate such symetry), the devices will work just as well if the source is biased with respect to a common point drain). Insight as to how said Schottky barrier MOSFETS might operate is provided in the Lepselter and Sze paper referenced in the Background Section. Briefly, said article considers that the source region junction of a P-channel device formed on N-type silicon, using platinum as the metalization, is reverse biased during operation and that it is reverse leakage or tunneling current which is modulated by the applied gate voltage. This article states that it was the source which was reverse biased during operation. Designation of source and drain, however, are dependent upon position within a circuit.

[0042] Reference to Figs. 6a & 6b and 7a & 7b show that N and P-channel MOSFET devices fabricated on P and N-type silicon respectively by the inventor herein, using approximately eight-hundred (800) angstroms of chromium as the metalization, which chromium was simultaneously vacuum deposited on both N (11) and P-type (12) silicon and then simultaneously vacuum annealed to said N (11) and P-type (12) silicon at four-hundred (400) degrees centigrade for thirty (30) minutes, provide MOSFET-type operational Drain Current vs. Drain-to-Source voltage curves as a function of Gate-to-Source voltage. It is also disclosed that tested devices demonstrated by Figs. 6a & 7a had a Gate (15a or 15b) length and width of approximately ten (10) microns and seventy-five (75) microns respectively, and that test devices demonstrated by Figs. 6b & 7b had a Gate length and width of approximately ten (10) microns and fifteen (15) mils respectively. It is noted that Fig. 6a and 6b Drain Current vs. Drain-to-Source Voltage curves for MOSFET devices, (as a function of gate-to-source volts), fabricated on P-type silicon (12), (ie. N-Channel Schottky barrier MOSFETS), are in the third quadrant and the Fig. 7a and 7b Drain Current vs. Drain-to-Source Voltage curves for devices, (as a function of gate-to-source volts), fabricated on N-type (11) silicon, (ie. P-Channel Schottky barrier MOSFETS), are in the first quadrant. The Drain Current flow direction is thus seen to be opposite to what would be expected by reference to the Lepselter et al. article referenced in the Background Section of this Disclosure regarding Schottky barrier MOSFETS, and opposite to that which occurs in Diffused Junction MOSFETS. That is, the present devices operate with the Drain junction in each device reverse biased rather than the Source junction, as was reported by Lepselter and Sze regarding the Schottky barrier MOSFETS they fabricated. At this time the mechanism of operation of the present invention MOSFETS represented by Figs. 6a & 6b and 7a & 7b is not fully understood, however it is believed that modulation of Reverse Bias Leakage Current through the Reverse Biased Drain Schottky barrier junction, as a result of applied Gate Voltage Modulated Semiconductor Doping, serves as an explanation as to what is occurring. This explanation is consistent with the well known fact that Schottky barrier junctions formed on more highly doped Silicon demonstrate a larger Reverse Bias Leakage Current than those formed on less highly doped Silicon and the known fact that application of a Gate Voltage in a MOSFET serves to modulate Effective Channel Region Doping. It is also noted and emphasized that the Drain-Current vs. Drain-to-Source Voltage Curves in Figs. 6a & 6b and 7a & 7b are quite Complementary and nearly symetrical with respect to one another. These attributes make the devices which provided said Drain-Current vs. Drain-to-Source Voltage Curves quite appropriate for application in combined CMOS device systems. It is also

noted that devices formed on both N (11) and P-type (12) silicon show a small drain current with zero (0.0) Gate-to-Source volts applied. Application of gate voltages of opposite polarities serve to reduce said Drain Currents to essentially zero in the respective MOSFET devices formed on N and P-type silicon respectively, however, making said devices initially depletion mode in nature. It is believed that partial Channel Region Inversion effected by applied Gate and Drain Voltages, or Gate Oxide Leakage Currents account for this effect. It is also reported that the onset of drain current conduction in present fabricated tested N-Channel Schottky barrier MOSFET devices has been found to correlate very well with Capacitance-Voltage (CV) plot onset of channel inversion, (which occurs at approximately minus (-4.0) volts in N-Channel devices, leading to the proposal that positive ions in the oxide may account for a shifted threshold of conduction and the presence of zero (0.0) gate-to-source volts drain current flow rather than poor oxide or gate uninfluenced drain current flow. It is also expressly pointed out that no Drain Current flow was detected in fabricated N or P-Channel MOSFETS when the Gate (15a or 15b) Voltage was of a polarity not appropriate to cause Channel Region Inversion, or when the same Polarity Voltage was applied from a Gate to Source and from a Drain to Source. That is, in fabricated N and P-Channel MOSFETS, Drain Current Curves were obtained only when the Applied Gate Voltage Polarity was appropriate to Invert a Channel Region, and when the Applied Drain to Source Voltage was of an Opposite Polarity to that Applied between said Gate to Source. This MOSFET Operational scenario is believed by the Inventor to be surprising and previously unreported. It is also believed that formation of a "Pinch-off" region in a Channel Region of a present invention Schottky barrier N or P-Channel MOSFET, when the Polarities of the Voltages applied to the Drain and Gate thereof are the same, serves to "shelter" the then Reverse-Biased Source Junction, and that insufficient Voltage Drop thereacross in use prevents the forcing of Reverse Bias Leakage Current therethrough. That is, the Pinch-off regions absorbs all applied Voltage. This, of course, does not occur where opposite polarity voltages are applied to the Gate and Drain of a MOSFET. In that case essentially all applied Voltage between a Drain and Source will drop across the reverse biased Drain, with the Source being forward biased. No Pinch-off Region will be present to absorb any of the applied Drain to Source Voltage. In contrast, it is noted that in conventional Diffused Junction MOSFETS the Pinch-off Region is responsible for causing Drain Current Saturation. That is, Operational Drain Current Curves achieved when a Pinch-off Region is present. It is also noted that the Schottky barrier MOSFETS reported by Koeneke et al. and by Legselter and Sze, referenced in the Background Section of this Disclosure, operate when a "Pinch-off" Region is present, (ie. when the same polarity voltages are applied to the Gate and Drain of their Schottky barrier MOSFETS), much as do conventional Diffused Junction MOSFETS. This is proven by the statement in the Koeneke et al. Patent to the effect that their reported Schottky barrier MOSFETS can replace conventional Diffused Junction MOSFETS in a circuit, and provide protection against Latch-up of a CMOS circuit when such is done. This point is emphasized to draw attention to the surprising nature of the operating characteristics of the present invention Schottky barrier MOSFETS, which Operating Characteristics make them suitable for use in forming a CMOS system which demonstrates Regenerative switching. No other known MOSFET provides Operating Characteristics which could effect Regenerative Switching in a CMOS System, emphasis added.

[0043] It is emphasized that the Drain-Current vs. Drain-to-Source-Voltage Operational Curves of present invention MOSFETS, (see Figs. 6a, 6b, 7a & 7b), are unlike those of Diffused Junction MOSFETS, or reported Schottky barrier MOSFETS. That is, significant Drain Current, (as a function of applied Gate Voltage), flow occurs only when the polarity of the applied voltages applied between a Gate (eg. 15a or 15b) and a Source (eg. 2b or 3a respectively), and that between a Drain (eg. 2a or 3b respectively) and Source, (eg. 2b or 3a respectively) are simultaneously of opposite polarities, and where the polarity of the Voltage Applied to the Gate, (eg. 15a or 15b respectively), is appropriate to effect an Inverted Channel Region in the type of Semiconductor involved. (Note, a Positive Potential Applied Gate Voltage will effect an N-Type Inversion Channel Region in P-type Silicon and a Negative Applied Gate Voltage will effect an Inversion P-Type Channel Region in N-Type Silicon).

[0044] Continuing, electrically interconnecting P-Channel MOSFET Source (2b) and N-Channel MOSFET Source (3a) as described above to form a CMOS device system, and sequentially, but simultaneously, varying values of Gate-to-Source voltage to electrically interconnected Gates (15a) and (15b), provides CMOS device system Regenerative Switching Operational Curves such as qualitatively shown in Fig. 8a.

[0045] Fig. 8a shows that the voltage (Vm), (ie. voltage present at the electrically interconnected point of P-Channel MOSFET Source (2b) and N-Channel MOSFET Source (3a), switches between, essentially that applied to Drain (2a) (ie. Vd1) and that applied to Drain (3b) (ie. Vd2) by external circuitry, when the Gate Voltage Applied simultaneously to P and N-Channel MOSFET Gates (15a) and (15b) is simultaneously varied between that applied to N-Channel MOSFET Drain (3b) (Vd2) and P-Channel MOSFET Drain (2a) (ie. Vd1). That is, a Voltage Inverting Switch occurs. It is noted that the nature of said inverting switch is "Regenerative", as discussed in the Disclosure of the Invention Section of this Disclosure. With reference to Figs. 3, 4, 8a and 8b however, it is again noted that the Sources (2b) & (3a) of the present invention Schottky barrier P and N-Channel MOSFETS are electrically interconnected to one another as are the Gates (15a) & (15b) thereof electrically interconnected to one another, to form a Regeneratively switching CMOS System. The Drain (2a) of the P-Channel MOSFET is then caused to be connected to a Positive Voltage (+Vd1) with respect to the Voltage (Vd2) applied to the Drain (3b) of the N-Channel MOSFET. Then, as shown in Fig. 8a, when the

electrically interconnected Gates (15a) & (15b) have applied thereto the relatively higher Voltage (+Vd1) applied to the Drain (2a) of the P-Channel MOSFET, the Voltage (VM) at the electrically interconnected P and N-Channel MOSFET Sources (2b) & (3a) is caused to Regeneratively switch (ie. invert), to essentially the lower Voltage (Vd2) applied to the Drain (3b) of the N-Channel MOSFET. When the Voltage applied to the electrically interconnected MOSFET Gates (15a) & (15b) is caused to be set to lower Voltage (Vd2), (eg lower with respect to that applied to the Drain (2a) of the P-Channel MOSFET), applied to the N-Channel MOSFET Drain (3b), the Voltage (VM) Regeneratively switches (ie. inverts) to essentially the relatively higher Voltage (Vd1) applied to the Drain (2a) of the P-Channel MOSFET. The reason the switching is Regenerative is that each MOSFET is turned "on" by applying Voltage between the Gate and Source thereof. In the present invention CMOS system, the Voltage at the electrically interconnected Sources changes during a switch, to a value which further encourages the switching in the MOSFET which is turning "on", and the more "on" a MOSFET becomes the further the Source Voltage moves in a direction which encourages greater Channel Inversion to take place. It is also noted that the Voltage (VM) which presents at the electrically interconnected Sources of the P and N-Channel MOSFETS of the present invention results from a voltage division between the effective impedances presented by the P and N-Channel MOSFETS. It is readily observable that said resistance provided by an "off" MOSFET is much greater than that provided by an "on" MOSFET, by referral to Figs. 6a, 6b and 7a, 7b. Essentially no current flow was observed in "off" MOSFETS

[0046] Fig. 8b shows a schematic diagram of a Regenerative CMOS Switching System of the present invention. Shown are electrically interconnected P-Channel and N-Channel MOSFET Gates (15a) and (15b) respectively, (which form a common Gate (G)), electrically interconnected P and N-Channel MOSFET Sources (2b) and (3a) respectively, (forming Midpoint (M)), and electrically noninterconnected P and N-Channel Drains (2a) and (3b) respectively with Applied Voltages VD1 and VD2 applied thereto respectively, where Vd1 is indicated as being positive with respect to Vd2. Also indicated are the presence of N-Type (11) and P-Type (12) Silicon in the P-Channel and N-Channel MOSFETS respectively.

[0047] Continuing, coupling drain (2b) and drain (3a) as described above to form a CMOS device system, and sequentially, but simultaneously, applying varying values of gate-to-source voltage to coupled gates (15a) and (15b) provides CMOS device system operational curves such as shown in Fig. 8a. (See Figs. 8b and 13b for a circuit symbol representation thereof). Fig. 8a shows the voltage (Vm), (ie. voltage present at the electrical interconnection connection point of drain (2b) and drain (3a), switches between, essentially, that (Vss) applied to source (2a) and that (-Vdd) applied to source (3b) by external circuitry, when the gate voltage applied simultaneously to electrically interconnected device gates (15a) and (15b) is varied. (See discussion of Fig. 13a (supra) for insight as to conventional diffused junction CMOS system operation and of Fig. 13b (supra) for additional insight to operation of Schottky barrier CMOS system operation).

[0048] It is specifically pointed out that the combination of N and P-Channel hot-carrier Schottky barrier junction MOSFETS to form a CMOS system which demonstrates Regenerative Switching, which N and P-Channel Schottky barrier MOSFETS have been shown to be fabricatable by a common procedure, is new novel and non-obvious. No known reference suggests that MOSFETS which operate only with opposite polarity voltages applied to the Gate and Drain are achievable. No known reference suggests that Chromium annealed to N or P-Type Silicon in a simultaneous process would form such MOSFETS. Discovery thereof by the Inventor was a surprise. Next, no known reference suggests that a CMOS System can be configured by electrically interconnecting the Sources of N and P-Channel MOSFETS, with the result that Regenerative Switching is demonstrated in use. The utility provided by the present invention is found not only in the resulting CMOS Systems achieved, but also in the ease of fabrication of CMOS Systems using Schottky barrier junctions in both N and P-Channel MOSFETS. Present invention CMOS systems, because of the use of hot-carrier Schottky barrier junctions, (rather than diffused junctions which involve switching speed reducing minority carriers), in both N and P-Channel MOSFET Source and Drain Regions, and because of the Regenerative nature of the switching provided thereby, (as dictated by the operational characteristics of both N and P-Channel Schottky barrier MOSFETS actually fabricated using Chromium as the Schottky barrier forming metal), can provide extremely fast, high frequency operational devices. It is also to be understood that the terms "operate" and "operational" are to be understood to mean that significant Drain Current modulation occurs when applied Gate Voltage is changed in a polarity direction which serves to invert a Channel Region in the presence of an opposite Polarity applied Drain Voltage, as represented by the third quadrant of Figs. 6a & 6b and the first quadrant in Figs. 7a & 7b. It is to be understood that while some relatively small currents may flow in other Polarity combination representing quadrants of said Figures, said other quadrants represent non-operational modes of applied Voltages Polarities.

[0049] It is also noted that it is possible to form a series combination of two, (N-channel or P-channel), MOSFETS to form transistor-load device systems or balanced differential MOSFET transistor pair systems. Such configurations can be N-channel device and N-channel load, P-channel device and P-channel load, N-channel device and P-channel load and P-channel device and N-channel load, (See Figs. 14, 15(a) and (15(b) for representative circuit symbol representations). In a transistor-load device system the source of one device is electrically interconnected to a drain of another and the gate of the load device is typically electrically interconnected to lead on the load device not connected to the

transistor. The gates of the transistor and load are not electrically interconnected and during use a voltage input signal is applied between tee free transistor gate and its source, while a load voltage is applied between the electrically interconnected load gate and the lead on the load transistor not electrically interconnected with the transistor, and the source of the transistor. In a balanced differential MOSFET transistor pair system the sources of two MOSFETS devices are electrically interconnected and the gates of the so interconnected devices are not directly electrically interconnected, but rather attach across a source of voltage. Each MOSFET drain is also attached to a source of voltage which is referenced to the electrically interconnected sources, normally through a load, and application of a voltage difference between the gates of the two MOSFET devices effects a current flow through the drains. It should be appreciated that only the voltage difference between said gates has an effect on current through said balanced differential pair system drains. That is, common-mode voltage applied to both gates has no significant effect on current flow through the device system MOSFET drains. The present invention should be considered to include such configurations as the distinction therein is the type of silicon upon which two simultaneously fabricated electrically interconnected devices are formed. That is, instead of electrically interconnecting MOSFET devices formed on N and P-type silicon, two devices formed on N-type, or two devices formed on P-type, silicon are electrically interconnected. Referring to Figs. 3 and 4, this would correspond to interpreting both semiconductor regions (11) and (12) to be of one type, (ie. N or P-type) to demonstrate a MOSFET with a MOSFET load, along with, typically, considering the shown common gate electrical connection as broken, and with an electrical connection added between the load device drain and gate, perhaps through a resistor. A simple seriesed MOSFET configuration is realized by electrically connecting a rectifying junction drain (2b) of one MOSFET to a rectifying junction source (3a) of another. As well, simply considering rectifying junctions (2b) and (3a) to be electrically connected sources and (2a) and (3b) to represent drains of devices formed in semiconductor regions (11) and (12) in Figs. 3 and 4, provides pictorial representation of the balanced differential MOSFET pair configuration. As mentioned above, in such a balanced differential MOSFET pair system the gates of the devices are not electrically interconnected and the shown electrical interconnection would be broken so that a voltage difference could be applied therebetween.

[0050] Continuing, (and of particular importance), if semiconductor regions (11) and (12) in Fig. 4 are considered to be of the same doping type, (ie. N or P or intrinsic), and metal (15) or a silicide in regions (2a) and (3b), provides rectifying junctions on said semiconductor (11) and (12), then applying gate volts (Vg) simultaneously to gates (15a) and (15b) can effect a single substrate type, (ie. single device), equivalent to CMOS. For instance, if semiconductor regions (11) and (12) are both N-type and a positive value of (Vdd) is applied to the rectifying junction at (3b) while a less positive voltage (Vss) is applied to rectifying junction (2a), then said applied voltages (Vdd) and (Vss) will cause the rectifying junction at (3b) to be forward biased and the rectifying junction at (2a) to be reverse biased. Application of a negative gate voltage to gates (15a) and (15b) just sufficient to cause onset of inverted channel regions thereunder in the semiconductor, in effect causes the rectifying junction at (3b) to become reverse biased and the rectifying junction at (2a) to become forward biased at said channel regions. That is, the reverse and forward biased rectifying junction positions are switched. It will be appreciated that if said forward biased rectifying junctions are not required or allowed to carry much current flow, which is effected by limiting the magnitude of the applied gate voltage and external loading connected at (2b) and (3a), the end effect will be to cause the voltage (Vm), as identified in Fig. 4, to shift between (Vdd) and (Vss). It is pointed out that it is preferable to effect an essentially non-rectifying contact for sensing (Vm) at (2b) and (3a). That is, the use of a different metal and/or silicide might be preferable in semiconductor regions (2b) and (3a) as compared to that utilized in semiconductor regions (2a) and (3b), said different metal and/or silicide serving to form non-rectifying rather than rectifying junctions with the semiconductor substrate at (2b) and (3a). The Semiconductor substrate (11) and (12) can also, or in the alternative, be caused to be of a doping level at (2b) and (3a) by diffusion or ion implantation for instance, so as to cause an effectively non-rectifying junction at (2b) and (3a) using the same metal and/or silicide that forms Schottky barrier rectifying junctions at (2a) and (3b). (Note that metal-semiconductor and metal-silicide-semiconductor junctions wherein the semiconductor is relatively highly doped, (eg. typically ten-to-the-eighteenth per centimeter cubed and higher), often demonstrate essentially non-rectifying current-voltage characteristics). As well, while introducing a high resistance region, use of a compensated essentially intrinsic semiconductor at the (2b) and (3a) regions can provide non-rectifying contacts to a metal deposited thereon, and will not form undesired rectifying junctions with adjacent regions of semiconductor which are doped metalurgically or by application of a gate voltage. In fact, the entire substrate can be intrinsic with N and P-type doping effected completely by applied gate voltages. This avoids the problem which can develop wherein a channel region accessing opening in a gate is sufficiently large that inverting channel voltage applied thereto can not serve to invert the channel region within the opening, thereby causing a rectifying junction between a doped semiconductor inverted channel and said channel accessing region. Where channel accessing regions are sufficiently small, this will not occur even in a doped semiconductor, and in fact reverse leakage current through such a rectifying junction, where it does exist, can make said semiconductor compensation unnecessary.

[0051] It will be appreciated that an equivalent single device CMOS system can also be effected on P-type semiconductor, wherein opposite polarity applied voltages (Vdd), (Vss) and (Vg) are utilized. In both cases, the required sub-

strate is of one type doping only. That is, formation of a checkerboard of alternating N and P-type doping regions is not required. emphasis added. The appropriate Claims are, in particular, to be interpreted to cover such single device equivalents to CMOS. It is also specifically noted that the electrically interconnected non-rectifying junctions in the CMOS type devices of the Honma et al. Patent cited in the Background Section herein are from opposite type semiconductor. The present invention device electrically interconnected non-rectifying junctions are on the same type material, emphasis added. It is also noted that non-rectifying junctions are easily achieved between aluminum and P-type silicon.

[0052] It is to be appreciated then, that the present invention can include devices in which Schottky barriers which are made essentially non-rectifying are present. It should also be understood that said Schottky barrier junctions which are made essentially non-rectifying do not have to be electrically interconnected connected, but could be represented by junctions (2a) and (3b), with junctions (2b) and (3a) being rectifying. This configuration on a single type substrate would, for instance, provide a balanced differential MOSFET pair in which, during operation, junctions (2b) and (3a) could be reverse biased and in which leakage current therethrough is controlled by application of appropriate semiconductor conductivity modulating gate voltages.

[0053] It is also mentioned that a voltage controlled switch can be configured from a MOSFET which has a rectifying Schottky barrier source junction, an non-rectifying drain junction, and a channel region therebetween, which channel region has an insulator and gate sequentially positioned adjacent thereto such that application of a voltage to said gate effects semiconductor doping in said channel region. That is, applying a positive voltage to the gate will attract electrons to the channel region and application of a negative gate voltage will attract holes to the channel region. Application of a voltage drain to source, such that the source junction is reverse biased, leads to little current flow. That is, only reverse bias Schottky barrier source current flows. By then applying a voltage between gate to source such that an inverted channel region is formed, a forward biased current through said source Schottky barrier junction can be effected. Such a voltage controlled switch is functionally a bit like a non-latching Silicon Controlled Rectifier (SCR). That is, forward current flow through a Schottky barrier can be started, and stopped, simply by the application of and removal of, a gate to source voltage. No known reference discloses such a configuration and use of a MOSFET device as described.

[0054] Figs. 9(a) through 9(k) demonstrate a preferred MOSFET fabrication process, including steps for providing isolation of devices via provision of relatively thick silicon dioxide therebetween. Fig. 9(a) shows a side view of silicon substrate (90). Fig. 9(b) shows said silicon substrate (90) in side view with relatively thick layer of silicon dioxide (91) grown atop thereof. Fig. 9(c) shows, in side view, said relatively thick layer of silicon dioxide (91) etched to the silicon (90) surface in the center region thereof. (Many such regions would be formed an a substrate in production setting). Fig. 9(d) shows a side view of a relatively thin layer of silicon dioxide (92) grown in said center region. This relatively thin layer of silicon dioxide (92) is of a depth appropriate for use as a gate oxide in a MOSFET, (eg. typically hundreds to thousands of Angstroms). Fig. 9(e) shows, in side view, the structure of Fig. 9(d) with a relatively thick layer of gate forming metal deposited thereover. Fig. 9(f) shows a top view of the structure shown in Fig. 9(e), with a photoresist (96) pattern atop the relatively thick layer of gate forming metal (93) atop said relatively thin layer of silicon dioxide (92). Shown are device drain (94) and source (95) regions separated by a gate oxide formed from said relatively thin layer of silicon dioxide (92). Fig. 9(g) shows the structure of Figs. 9(e) and 9(f) in which said relatively thick layer of gate forming metal (93) and the relatively thin layer of silicon dioxide (92) have been etched to expose the underlying silicon substrate, prior to removal of the photoresist (96). Note that while not shown, a silicon substrate etch can also be performed at this point and be within the scope of the present invention preferred fabrication method. Such a silicon etch would provide a structure appearing much as shown in Figs. 3 and 4. Fig. 9(h) shows the structure of Fig 9(g) with the photoresist (96) removed and with a relatively thin layer of silicide forming metal (97) deposited thereover. Fig. 9(i) shows the structure of Fig. 9(h) after a silicide (98) forming anneal, and an etch which removes any remaining silicide forming metal (97). Note that the etchant is selected so as not to adversely effect the relatively thick layer of gate forming metal, but so that it serves to remove any remaining thin layer of device drain (94) to source (95) shorting silicide forming metal on the etched, gate insulator forming, sides of the relatively thin layer of silicon dioxide (92). This is the case even where the relatively thick layer of gate forming metal and the relatively thin layer of silicide forming metal are the same element. It has been found, however, that Aluminum is a good element for use as a relatively thick gate forming metal (93) and that Chromium is a good relatively thin layer of silicide forming metal (97) element for use on either N or P-type silicon. This is in part because a chromium etchant comprised of cerric ammonium nitrate, (eight (8) grams), and perchloric acid, (three (3) milliliters), in deionized water, (forty (40) milliliters), is effective in etching chromium but essentially ineffective in etching Aluminum, and in part because Aluminum adheres well to silicon dioxide after deposition in a sputtering chamber. Unless done with a substrate held at an elevated temperature, deposited Chromium on silicon dioxide does not always adhere so well, with water necessary in subsequent processing steps serving to "crinkle" said Chromium off of said silicon dioxide. Fig. 9(j) shows the structure of Fig. 9(i) but with the relatively thick layer of gate forming metal (93), over the relatively thick layer of silicon dioxide (91), removed. An additional but simple photoresist procedure accomplishes this when desired. In fact, the same mask used to effect etching of the relatively thick layer of gate forming metal and silicon dioxide as represented in Fig. 9(c), can be used at this point, coupled with use of an opposite type photoresist, (eg. positive photoresist instead of negative photoresist). The above sequence of Figures demonstrates a preferred

method of fabricating the MOSFET devices of the present invention. Fig. 9(k) represents a structure as in Fig. 9(i), but in which the silicon substrate (90) is comprised of two different dopings, (90a) and (90b) within one MOSFET device region. Said two dopings (90a) and (90b) could be of the same type, or of opposite (eg. N and P-type), types. Fig. 9(l) shows two MOSFETS on one substrate, each fabricated entirely over a doping single level or type of silicon, (ie. (90c) and (90d). If the doping types (90c) and (90d) are of opposite type this represents a CMOS structure. Fig. 9(m) shows a structure in which junction regions from two adjoining MOSFET structures are merged. It is again mentioned that the type of, and level of, doping of a semiconductor substrate annealed to a metal to form a junction determine the electrical characteristics of said formed junction. Annealing chromium at approximately four (400) to five (500) hundred and above degrees centigrade to either N or P-type silicon, doped to levels below about ten-to-the-sixteenth per centimeter cubed, provide rectifying junctions on both silicon types. Annealing chromium to silicon of either type doped approximately ten-to-the-eighteenth and above per centimeter cubed, provides junctions with essentially non-rectifying characteristics. Hence, controlling the type and the level of doping of silicon to which chromium is annealed can provide junctions with a wide variety of electrical characteristics. Metals other than chromium can also be utilized. As described earlier in this Disclosure, this enables production of a variety of devices.

[0055] Next, Figs. 10(a) through 10(i) demonstrate a preferred fabrication procedure for a non-inverting single device equivalent to CMOS, which is fabricated on a single substrate type. Note that only device forming steps are shown and it is to be assumed that device separation can be provided similar to as shown in Figs. 9(a) - 9(d). Fig. 10(a) shows a side view of a silicon substrate (100). Fig. 10(b) shows silicon dioxide (102) grown atop said silicon substrate (100) and Fig. 10(c) shows a layer of gate forming metal (106) deposited atop said silicon dioxide (102). Fig. 10(d) shows a top view of source (104) and drain (105) openings are made to the silicon (100) through gate forming metal (106) and silicon dioxide (102). Fig. 10(e) shows a side view of the same openings shown in Fig. 10(e). Fig. 10(f) shows a layer of silicide forming metal (107) deposited over the silicon substrate (100). Fig. 10(g) shows the presence of silicide (108) formed after an anneal procedure which, when chromium is utilized can be four-hundred-fifty (450) degrees centigrade for thirty (30) minutes. Fig. 10(h) shows a top view of the substrate of Fig. 10(g) but with a channel accessing opening (110) also present, etched through the gate forming metal (106) and silicon dioxide (102). Fig. 10(i) shows a side view thereof taken at b--b in Fig. 10(h). Note that in said side view of Fig. 10(i) the structure is validly described as two MOSFETS with one Schottky barrier, (with non-rectifying characteristics), of each being electrically interconnected, very much as shown in Fig. 4. (Note, in Figs. 9(a) through 9(m) and Figs. 10(a) through 10(i) no etch is shown into semiconductor substrates (90) and (100) as are shown in Figs. 3, 4 and 5. Said semiconductor etch is optional. It is noted that the silicon substrate (100) can be intrinsic, N-type or P-type and that silicon channel region in opening (110) can be intrinsic or oppositely doped, even where the silicon substrate (100) is N or P-type. It is noted that opening (110) might be two openings, the silicon under one being heavily doped N-type and heavily doped P-type in the other to enhance non-rectifying contact to the silicon channel region in both the metalurgical and inverted state, however, such is typically unnecessary because leakage current through even a reverse biased junction will allow a voltage to be monitored in the channel through a reverse biased junction. It is noted that testing of fabricated devices tends to verify this conclusion. Where the hole (110) is sufficiently small fringing of an electric field due to a voltage applied to the gate will serve to invert the silicon channel region even under the hole (110), and a junction between inverted and noninverted silicon in the silicon channel region under the hole (110) will not exist. It should be clear in view of the foregoing that single device equivalent to CMOS can be considered as two MOSFETS formed on the same type semiconductor, with non-rectifying drain junctions interconnected. At this point it is specifically pointed out that while the Honma et al. Patent, the closest known art and cited in the Background Section herein, shows a CMOS device system in which non-rectifying drain junctions are interconnected, said non-rectifying drain junctions are to N-type silicon in one device and to P-type silicon in the other of two electrically interconnected devices. That is, the CMOS structure presented requires the presence of both N and P-type silicon. This is an extremely important contrasting distinction regarding the present invention, in which only a single substrate type (ie. N-type, P-type or intrinsic), is required, emphasis added. That is, the costly steps associated with forming an alternating checkerboard of N and P-type regions in a substrate common to all known CMOS devices are not necessary.

[0056] Testing of fabricated non-inverting single device equivalents to CMOS has surprizenly shown that application of a voltage from drain to source without any gate voltage being applied provides no voltage at the midpoint channel accessing region with respect to source, where intrinsic silicon was utilized. Applying a voltage gate to source provides a voltage present at said midpoint channel accessing region. This occurs whether drain and source are provided positive or negative voltage with respect to source.

[0057] Continuing, Figs. 10(j) through 10(r) demonstrate a fabrication procedure for an inverting single device equivalent to CMOS. The fabrication process is similar to that described above for a non-inverting single device equivalent to CMOS but the end result is configured so that silicide (108) is present in the silicon at the center opening (110) rather than in the equivalent source and drain regions (104) and (105). Also shown is a delineating guard-ring of silicide (108) around the device which serves to help reduce leakage currents. Fig. 10(j) shows a silicon substrate (100). Fig. 10(k) shows silicon dioxide (102) grown atop the silicon substrate (100). Fig. 10(l) shows gate forming metal (106) deposited

atop said silicon dioxide (102). Fig. 10(m) shows center opening (110) etched through the gate forming metal (106) and silicon dioxide (102) to provide access to the silicon substrate (100) surface. Fig. 10(n) is a cross sectional view taken at c--c in Fig. 10(m). Fig. 10(o) shows a layer of silicide forming metal (107) deposited over the substrate of Fig. 10(n). An anneal then causes silicide (108) to form where the silicide forming metal (107) is in contact with the silicon substrate (100) at the midpoint (110) opening. Fig. 10(p) shows all remaining silicide forming metal (107) removed. Fig. 10(q) shows source and drain regions (104) and (105) opened to the silicon substrate (100) surface. Fig. 10(r) is a cross sectional view taken at d--d in Fig. 10(q). It will be appreciated that there are actually two, first and second, channel regions present in this device because the Schottky barrier rectifying junction is situated between two non-rectifying, (ie.conductive) junctions. The first and second channel regions are between drain (105) and midpoint (110), and between source (104) and midpoint (110) respectively. Note that the drain (105) to midpoint (110) silicide (108) can be effectively replaced by a resistor, but that such is not optimum as when the midpoint (110) silicide (108) to source (104) Schottky barrier junction is caused, by gate applied volts, to become forward biased, no reverse biased junction then exists to limit current flow drain (105) to source (104) to a reverse bias Schottky barrier junction level. For the purpose of Claim construction such a configuration is to be considered but a case of a Schottky barrier which demonstrates non-rectifying essentially ohmic characteristics as a result of semiconductor doping and the like.

[0058] A bit of reflection should make it clear that application of a gate voltage to the device of Fig. 10(i) is necessary to effect a rectifying Schottky barrier drain (105) to source (104) applied voltage, at an non-rectifying midpoint (110) location. Say for instance the silicon substrate (100) is P-type and positive voltage is applied to rectifying Schottky barrier drain (105) with respect to source (104). Said rectifying Schottky barrier drain (105) junction will be reverse biased, said rectifying Schottky barrier source junction (104) will be forward biased. As a result no voltage appears at midpoint (110). Application of a positive gate to source voltage will invert the silicon in the channel region to N-type, thereby causing the rectifying Schottky barrier midpoint drain and source junctions to become forward and reverse biased respectively, thereby effecting a voltage at non-rectifying midpoint (110).

[0059] A constant polarity drain (105) to source (104) applied voltage present at rectifying Schottky barrier midpoint (110) in the device of Fig. 10(r) however, will be caused to be reduced by application of a gate to source (104) voltage. For instance if the silicon substrate (100) is P-type, application of a positive voltage at non-rectifying drain (105) will cause said applied positive voltage to appear through forward biased rectifying Schottky barrier midpoint (110) junction through non-rectifying drain (105) with no gate volts applied with respect to non-rectifying source (104), said positive volts appearing across reverse biased rectifying Schottky barrier midpoint (110) junctions to the source (104). Application of positive gate volts with respect to non-rectifying source (104) will invert the silicon in the channel regions and cause the rectifying Schottky barrier midpoint (110) junction to the non-rectifying drain (105) to become reverse biased, and the rectifying Schottky midpoint (110) barrier to the non-rectifying source (104) to become forward biased, thereby lowering said midpoint (110) voltage.

[0060] It is to be understood that while the non-inverting and inverting embodiments are shown with channel physically between two Schottky barrier junctions, and with Schottky barrier junctions physically between two non-rectifying junctions respectively, such is demonstrating and limiting. For instance, the channel region in the non-inverting embodiment could be physically split into two parts which are electrically interconnected and the Midpoint Schottky barrier junctions in the inverting embodiment could be located non-centrally but electrically interconnected. This could occur, for instance, if two separate devices are involved or if physical layout on a single substrate is changed. Functionally equivalent
embodiments to any device or device system demonstrated in this Disclosure are within the scope of the present invention and appropriate Claims.

[0061] Figs. 11ao - 11go, 11a1 - 11g1, 11a2 - 11g2p and 11a3 - 11g3, there are shown generally similar approaches to forming Schottky barrier junctions which can be incorporated into the Schottky barrier junction based systems demonstrated by Figs. 9a - 9m and Figs. 10a - 10i. The reason for incorporating such is to limit the area of Schottky barrier junction to the minimum necessary to provide a channel region current, but minimize leakage current to a semiconductor substrate from a drain.

[0062] Figs. 11ao, 11a1, 11a2, and 11a3 show a silicon substrate (100), and Figs. 11bo, 11b1, 11b2 and 11b3 show a silicon dioxide grown (102) atop thereof. Fig. 11c0 shows the substrate of Fig. 11bo with the silicon dioxide (102) and silicon (100) etched anisotropically and isotropically respectively. Said silicon is etched to an underlying insulating substrate (SUB). Fig. 11c1 is the substrate of Fig. 11b1 with the silicon dioxide (102) and silicon (100) etched anisotropically and isotropically respectively. Figs. 11c2 and 11c3 show the substrates of Figs. 11b2 and 11b3 with both the silicon dioxide (102) and silicon (100) etched anisotropically. It should be understood that isotropic etching is commonly achieved by a wet acid technique, and that anisotropic etching is typically achieved by dry plasma techniques. Figs. 11do is Fig. 11co repeated to hold the place in the sequence alongside the other drawings. Figs. 11d1, 11d2 and 11d3 show insulating silicon dioxide (102) grown and etched in the etched silicon (100) regions. Note that Fig. 11c3p shows a diffused region (100d) which can serve to effect an essentially non-rectifying junction rather than a Schottky barrier junction with a deposited silicide forming metal (107) as shown in Figs. 11e0, 11e1, 11e2 and 11e3. It is best to deposit

said silicide forming metal by a non-line-of-sight technique such as sputtering, when an undercut surface silicon dioxide device geometry is present so that said silicide forming metal can be deflected to the source and drain ends of said silicon channel. This is in contrast to the line-of-site deposition approach required in devices with geometries such as demonstrated in Figs. 3 and 4. After a silicide forming anneal (eg. 450 degrees centigrade for 30 minutes if chromium and silicon are utilized), all remaining silicide forming metal (107) is removed by an etching procedure, leaving silicide regions (108) in place, as shown in Figs. 11fo, 11f1, 11f2 and 11f3. It is to be appreciated that the silicide (108) regions are present only adjacent to the ends of channel regions, thus the leakage currents, being proportionate to junction area, are reduced to essentially a minimum, emphasis added. Figs. 11go, 11g, 11g2 and 11g3 show conductor metal (103), (eg. typically aluminum), applied and etched to provide contact to the Schottky barrier junction regions (108), and to provide gate metalization. Note that Fig. 11g2p shows a variation wherein the silicon dioxide (102) covers even more of the etched silicon (100) region.

[0063] Figs. 11ha, 11hb, 11i, 11j and 11k show Schottky barrier MOSFETS with Source, Drain and Gates identified, fabricated to include the insulating material achieved low leakage Schottky barrier device geometries as just described. Devices fabricated as just described eliminate a large portion of the Schottky barrier junction area such shown as present in Figs. 3 and 4 between the metal (15) and semiconductor (11) and (12). It is also to be noted that the Schottky barrier junction in, for instance, Fig. 11g0 and 11g1 are, as a consequence of the isotropic etching of the silicon (100), placed under a gate metalization. This eliminates another source of nonoptimum, current limitation in that during operation no high resistance gap exists between a gate voltage applied induced channel in the silicon and the Schottky barrier at the source and drain ends of said channel region. The present Schottky barrier devices then overcome both high leakage current and high effective channel region to source and drain gap induced resistance problems. Said problems were the focus in the Patent to Koeneke et al, No. 4,485,550, which Patent described the use of source and drain ion implantations as an approach to the overcoming thereof.

[0064] Figs. 11l, 11n and 11o show non-inverting single device equivalents to CMOS and Fig. 11m shows an inverting version. The same identifying numeral system is used in Figs. 11ha to 11o as was used in Figs. 11a0 to 11g3.

[0065] It is also within the scope of the present invention to effect selected insulated regions in an etched silicon source or drain region by deposition of a material, (eg. silicon nitride), which protects a silicon region during an oxidation procedure, then remove said protective material after said oxidation procedure. As well, a deposited nonoxide insulator in an etched semiconductor region might be allowed to remain with portions thereof etched away at ends of a channel region to allow silicide formation thereat. Such approaches might provide better results than simply growing oxide and etching it away where desired, particularly where gate silicon dioxide is undercut by an isotropic silicon etch, because selective etchants could be utilized to avoid adversely affecting an undercut oxide geometry.

[0066] Turning now to Figs. 12(a) and 12(b) there are shown circuit symbols for conventional diffused junction P-Channel and N-Channel MOSFET devices. The directions of the arrowheads on the line representing the substrate identify the MOSFET device type. (It is noted that the substrate is shown electrically interconnected to the source in Figs. (12a) through (15b). This is not to be considered absolutely required for a conventional or Schottky barrier MOSFET to operate, but simply observes conventional symbolism). In use the Drain (D) junction is considered reverse biased and a negative/(positive) voltage is applied to the gate (G) of a P-Channel/(N-Channel) device respectively. Application of a positive or negative voltage to a gate causes carriers, (ie. electrons or holes respectively), to accumulate at the semiconductor-insulator, (in the case of silicon an oxide is a typical insulating material), interface channel region in the semiconductor thereby forming a channel between source and drain. When the semiconductor is P-type and a positive gate voltage is applied, a conducting inverted N-type channel will form. When the semiconductor is N-type and a negative gate voltage is applied, a conducting inverted P-type channel will form.

[0067] Fig. 13a shows a conventional diffused junction MOSFET CMOS device system. Application of a gate voltage to interconnected gates (G) near positive (+Vdd) causes the N-Channel device to turn "on", (ie. form a conducting channel between its source (S) and drain (D)), while the P-Channel is turned "off" (ie. has no conducting channel between source and drain), thereby effecting a voltage near ground potential at the interconnected drains (D) point (M). Application of an essential ground potential to interconnected gates (G) causes the P-Channel device to turn "on", (while the N-Channel device is "off"), thereby effecting a voltage near positive (+Vdd) at said interconnected drains (D) midpoint (M).

[0068] Continuing, it must be understood that the present Schottky barrier MOSFETS operate differently than do conventional diffused junction MOSFETS in that applied Gate voltage effect on channel region substrate doping serves to modulate the leakage current through a reverse biased Schottky barrier junction. An effectively higher channel region doping serving to cause an increased reverse leakage current rather than simply effect a conducting similar type of doped semiconductor between source and drain. This difference in operational basis causes the voltage which must be applied between a drain and source of a Schottky barrier MOSFET to be opposite to that applied in a conventional diffused junction MOSFET. That is, current flows in the opposite direction in a Schottky barrier MOSFET as compared to a conventional diffused junction MOSFET of the same channel type, (ie. N-Channel or P-Channel). The following table demonstrates the voltage polarity comparisons in a clear concise manner:

MOSFETS				
	DIFFUSED JUNCTION		SCHOTTKY BARRIER	
	GATE	DRAIN	GATE	DRAIN
P-TYPE SUB. N-CHANNEL	+	+	+	-
N-TYPE SUB. P-CHANNEL	-	-	-	+

[0069] It is noted that operational gate voltage (Vg) polarity is the same for both diffused junction and Schottky barrier MOSFET technologies as negative/(positive) gate volts attract holes/(electrons) to a channel region in a semiconductor channel region. However, the operational applied drain voltage (-Vdd), as identified above, is reversed comparing conventional diffused junction and Schottky barrier MOSFETS. Fig. 13b is shown with the position of N-Channel and P-Channel devices reversed in a Schottky barrier CMOS system, but note that the Vdd is negative. The P-Channel Schottky barrier MOSFET could be placed as in Fig. 13a, if Vdd is made positive (ie +Vdd). Fig. 13b shows the configuration using the same circuit symbols as used for conventional diffused junction MOSFETS, but with a (SB) included to indicate that Schottky barrier junction technology is utilized in both source and drain. With a gate voltage (Vg) near Vss applied to the interconnected gates (G), the N-Channel device will have an effectively positive voltage applied thereto between its gate (G) and source (S). This will attract electrons to, and cause inversion of, the channel region therein, causing the Schottky barrier drain (D) junction electrically connected to the -Vdd to be reverse biased but conduct a gate controlled leakage, (ie. tunneling), current therethrough. The drain (D) of said N-Channel device will be reverse biased in the inverted channel region thereby providing a voltage (Vm) at the mid-point interconnected sources (S) of the N-Channel and P-Channel devices to be at essentially (-Vdd). Note that while the inverted channel in the N-Channel device is conducting, the channel in the P-Channel device does not conduct and is "off". This is confirmed by the curves shown in Figs. 6a, 6b and 7a, 7b, which curves were derived by test of actual fabricated P-Channel and N-Channel Schottky barrier MOSFETS. It is believed that energy band pinning in the channel region accounts for this result. That is, a noninverted channel region seems to be prevented from accumulating and therefore does not form a reverse bias conducting Schottky barrier junction with an applied source (or drain) region metalization, as does an inverted channel region. This point is subject of continued investigation. Continuing, when the gate voltage (Vg) is caused to be near (-Vdd), it should be appreciated by symetry that the N-Channel device will be "off" and that a conducting inverted P-Channel will be effected in said P-Channel device. That is, an effective negative voltage applied to the interconnected gates (G) attracts holes to the channel region of the P-Channel Schottky barrier device causing channel region substrate type inversion. This of course, effects a voltage (Vm) very near Vss at the mid-point interconnection of sources (S) as the drain Schottky barrier junction in the inverted channel region of the P-Channel device is effectively reverse biased with respect to the source voltage applied thereto. It is to be understood the that Vss in Fig. 13b can be replaced by a ground and the device system will still work. It is elaborated in the Disclosure of the Invention Section of this Specification that the switching in the circuit of Figs. 8b and 13b is regenerative, as it is the effective sources (S) of the N and P-Channel Schottky barrier MOSFETS which are electrically interconnected in use, rather than the drains (D) as in conventional diffused junction MOSFETS as shown in Fig. 13a.

[0070] (Note that the Lepselter and Sze article cited, and incorporated by reference infra herein, states that it was the source, in their Schottky barrier MOSFETS which was reverse biased during operation. The Schottky barrier MOSFETS fabricated by the Applicant, however, operated with the drain reverse biased. In the MOSFET devices reported by Lepselter and Sze, the same voltages polarities would be applied to the gate and drain as applied in conventional diffused junction MOSFETS and the drains of the N and P-Channel MOSFETS would be electrically interconnected, As well, the switching would not be regenerative).

[0071] Fig. 8a represents the gate voltage influence on voltage at midpoint (M) connection of the drains (D) of the N-Channel and P-Channel devices shown in Figs. 8b and 13b.

[0072] Fig. 14 shows circuit symbols for Schottky barrier MOSFETS of the same channel type, (shown P-Channel but simply changing device type indicating arrowhead direction represents N-Channel as well), configured in a balanced differential system such as commonly found in operational amplifiers. Note that nonsemiconductor components of Schottky barrier source junctions are electrically interconnected to effect the configuration. Also note that the gates are not electrically connected, but will connect across a source of voltage.

[0073] Figs. 15(a) and 15(b) show circuit symbols for N-Channel Schottky barrier MOSFETS configured in an active device with MOSFET load system. In Fig. (15a) the load is an N-channel MOSFET and in Fig. (15b) the load is a P-channel MOSFET. Similar systems can be configured using P-Channel Schottky barrier active device MOSFETS with MOSFET loads and Figs. (15a) and (15b) can be considered to show said arrangements by assuming the device type indicating arrowheads reversed.

[0074] Figs. 16a and 16b show coined circuit diagrams for present invention inverting and non-inverting, respectively, single device equivalents to CMOS. Identifiers (104), (105), (110), and (106) from Figs. 10i, 10q and 10r are indicated to provide a physical correspondence.

[0075] It is to be noted that Schottky barrier junctions are comprised of nonsemiconductor and semiconductor components, such as a (metal and/or metal silicide), and silicon respectively. Functional electrical interconnection of two Schottky barrier junctions is typically effected by connecting the nonsemiconductor components of two Schottky barrier junctions. Electrical interconnections can be achieved by conducting traces on a substrate, or by external wiring which accesses the nonsemiconductor component. It can occur that a common semiconductor area between two devices can effect a semiconductor electrical interconnection as well. In such a case a contact metal can be considered a nonsemiconductor "electrical interconnection" component. Also, the channel regions of Schottky barrier MOSFETS are formed in semiconductor and are typically continuous between respective rectifying source and drain junctions. That is, nonsemiconductor components of a Schottky barrier junction typically "sandwich" a "continuous" semiconductor channel region, which has an insulator and gate progressively situated atop thereof, therebetween. Also "respective" rectifying source and drain junctions are those rectifying junctions associated with a semiconductor channel region. As well, Schottky barrier junctions are typically assumed to be rectifying. It can occur, however, that a Schottky barrier can be made to demonstrate non-rectifying characteristics. Formation on heavily doped semiconductor, for instance, can provide this result. In the Claims, the term "non-rectifying" will be used to identify Schottky barrier junctions which demonstrate other than rectifying characteristics, said other characteristics typically being ohmic.

[0076] It is also to be understood that while Schottky barrier junctions are typically formed between a metal and a semiconductor or a metal-compound, (eg. silicide where silicon is utilized), and a semiconductor, the terms "metal forming silicide", in the case where the semiconductor is silicon, should be interpreted broad enough to include any material which forms a rectifying junction with a semiconductor, whether technically a metal or not, for the purposes of Claim interpretation.

[0077] It is noted that a Hewlett-Packard 4145B Parameter Analyzer was utilized to make measurements in experimental work reported in this Disclosure.

[0078] It is also noted that MOSFET devices formed on N-type semiconductor and which operate when a channel region is inverted are termed P-Channel devices. Likewise, MOSFET devices formed on P-type semiconductor and which operate when a channel region is inverted are termed N-Channel devices. That is, N-Channel MOSFET devices are formed on P-type semiconductor and P-Channel MOSFET devices are formed on N-type semiconductor. The reader should not be confused by this and in reading the Claims should keep this distinction clearly in mind.

[0079] The terminology "Single device equivalent to CMOS" has been used in the Disclosure because it draws attention to important similarities between the present invention devices and CMOS, where the present invention involves one MOSFET-like device formed on a single type semiconductor, in place of two electrically interconnected MOSFET devices in series as required in conventional diffused junction CMOS. For the purpose of Claim construction however, the terminology "single device with operating characteristics similar to CMOS" will be utilized".

[0080] Also, it is to be clear that when it is stated that a present invention device is formed on a "single-type" semiconductor, the intended meaning is that there is no requirement for a checkerboard of alternating N and P-type regions in a semiconductor to effect a single device with operating characteristics similar to conventional diffused junction CMOS device systems. It does not mean that regions of a single device of the present invention formed on N or P-type semiconductor can not have opposite type doping or intrinsic semiconductor present therein, or that single devices of the present invention formed on intrinsic semiconductor can not have regions of doped semiconductor present, or that a checkerboard of N and P-type regions, with single devices of the present invention in said regions can not be present, emphasis added. It means only that each present single device which provides operating characteristics similar to conventional diffused junction CMOS multiple device systems is formed in a single type semiconductor and that there is no requirement that a device formed in N-type semiconductor be electrically interconnected to a device formed in P-type semiconductor to provide the CMOS operating characteristics. The use of the terms "single device" should be taken to sufficiently distinguish over conventional diffused junction CMOS device systems which require both an N and a P-Channel device, be present with their drains electrically interconnected in series to provide a CMOS device system which demonstrates similar operating characteristics to a single device of the present invention.

[0081] In the Claims, it will be appreciated that when a Schottky barrier CMOS device system is described as resulting from electrical interconnection of present invention N and P-Channel Schottky barrier MOSFETS devices, the geometry of the Schottky barrier-channel region is well identified as providing Schottky barriers only at the end(s) of a channel region, which geometry serves to reduce leakage current problems, and this distinguishes over known prior art in mul-

tiple present invention device systems.

[0082] It is also noted that rectangular source and drain geometry was used for demonstrative, not limiting, purposes in the foregoing. Circular geometry, wherein a source region is essentially surrounded by a drain region for instance is to be considered equivalent and within the scope of the present invention.

[0083] It is to be understood that the terminology "Applied Drain and Source Voltages", as used in this Disclosure refer to voltages applied to a metal side of Schottky barrier junctions.

[0084] It is also noted that the Source and Drain junctions of a Schottky barrier MOSFET are physically typically indistinguishable from one another. That is, it is location in a circuit, and Applied Voltages which serve to identify a Source and Drain in an operating circuit. The Source being a Common Terminal with respect to which Gate and Drain Voltages are applied. This being the case, in the Claims the terminology "electrically interconnected" and electrically noninterconnected" are utilized to describe, for instance, "Schottky barrier Drains" and "Schottky barrier Sources" in a Regenerative Switching CMOS configuration. Said functional based language is equivalent to stating that in a Regenerative Switching CMOS System of the present invention, it is the Sources which are electrically interconnected and the Drains which are left free to be connected to Voltage Sources.

[0085] Having hereby disclosed the subject matter of the present invention, it should be obvious that many modifications, substitutions, and variations of the present invention are possible in light of the teachings. It is therefore to be understood that the present invention may be practiced other than as specifically described, and should be limited in breadth and scope only by the Claims.

Claims

1. An inverting single Metal Oxide Semiconductor (MOS) device with operating characteristics similar to multiple device Complimentary Metal Oxide Semiconductor (CMOS) systems and which can be used as a modulator, in which an applied gate (G) voltage controls a voltage present at an essentially electrically isolated terminal (M) thereof; comprising first and second essentially non-rectifying channel region junctions in a surface region of a single doping type semiconductor (100) selected from the group consisting of N-type, P-type, Intrinsic, N-type and Intrinsic, P-type and Intrinsic, N-type on insulator, and P-type on insulator, said first and second essentially non-rectifying channel region junctions being separated by first and second semiconductor (100) channel regions from electrically interconnected rectifying Schottky barrier to channel region junctions, wherein first and second gates (G) to which semiconductor (100) channel region doping type effecting modulating gate voltage (Vg) can be applied are associated with said first and second semiconductor (100) channel regions, said first and second gates (G) being offset from said first and second semiconductor (100) channel regions, respectively, by insulating material (102), such that application of a sufficient negative voltage (Vg) to the first and second gates (G) will attract holes into said first and second semiconductor (100) channel regions, and such that application of a sufficient positive voltage (Vg) to the first and second gates (G) will attract electrons into said first and second semiconductor (100) channel regions, the purpose of applying such gate voltage (Vg) being to modulate the effective doping type of said first and second semiconductor (100) channel regions, such that when a constant polarity voltage (Vd) is applied between said first and second essentially non-rectifying channel region junctions one rectifying Schottky barrier to channel region junction forward conducts while the other simultaneously does not, which Schottky barrier to channel region junction forward conducts at a specific time being determined by semiconductor (100) doping type in said first and second semiconductor (100) channel regions, said semiconductor (100) doping type being determined by applied gate voltage (Vg) polarity, which essentially electrically isolated terminal (M) electrically contacts, via a junction thereto, said electrically interconnected rectifying Schottky barrier to channel region junctions between said first and second semiconductor (100) channel regions and during use monitors a constant polarity voltage applied to one of the first and second essentially non-rectifying channel region junctions, which constant polarity voltage appears at said essentially electrically isolated terminal (M) essentially through the forward conducting Schottky barrier to channel region junction, which constant polarity voltage monitored by said essentially electrically isolated terminal (M) decreases when the gate voltage (Vg) applied to said first and second gates (G) is increased; the basis of operation being that said Schottky barrier junctions are formed between said first and second semiconductor channel regions and a material (108) which provides a rectifying junction to a semiconductor (100) channel region when it is doped either N or P-type.

2. An inverting single Metal Oxide Semiconductor (MOS) device with operating characteristics similar to multiple device Complimentary Metal Oxide Semiconductor (CMOS) systems as in Claim 1 in which at least one of said Schottky barrier to channel region junctions is formed in a region etched into said semiconductor (100), said etched semiconductor (100) being partially comprised of insulating material (102), the purpose thereof being to reduce leakage current by limiting the area of Schottky barrier to channel region junctions in contact with said semiconductor to regions at ends of said semiconductor (100) channel regions.

3. An inverting single Metal Oxide Semiconductor (MOS) device with operating characteristics similar to multiple device Complimentary Metal Oxide Semiconductor (CMOS) systems as in Claim 1 in which the semiconductor (100) is silicon and the Schottky barrier to channel region junctions are formed between said silicon (100) and at least one material (108) selected from the group consisting of chromium, molybdenum, tungsten, vanadium, titanium, platinum and a silicide of any thereof.

4. A method of configuring an Metal Oxide Semiconductor (MOS) device with operating characteristics similar to Complimentary Metal Oxide Semiconductor (CMOS) systems and which can be used as a modulator, comprising the steps of:

a. providing two Metal Oxide Semiconductor Field Effect Transistor (MOSFET) devices, each formed in a surface region of the same single doping type semiconductor selected from the group consisting of N-type, P-type, Intrinsic, N-type and Intrinsic, P-type and Intrinsic, N-type on Insulator, and P-type on Insulator, one said (MOSFET) device comprising two junctions, termed source and drain, separated by a first semiconductor (100) channel region, and the second (MOSFET) device comprising two junctions, termed source (S) and drain (D), separated by a second semiconductor (100) channel region, wherein gates (G) to which semiconductor (100) channel region inverting voltage (Vg) can be applied are associated with each of the first and second semiconductor (100) channel regions are offset from said first and second semiconductor (100) channel regions by insulating material (102), such that during use application a sufficient positive voltage (Vg) to said gates (g) will attract electrons to said first and second semiconductor (100) channel regions, and such that application of sufficient negative voltage (Vg) to said gates (G) will cause attraction of holes to both of said first and second semiconductor (100) channel regions, the purpose of applying such gate voltage (Vg) being to, modulate the effective doping type of said first and second semiconductor (100) channel regions between respective source (S) and drain (D) junctions, which source (S) junctions are each essentially non-rectifying, and which drain (D) junctions are rectifying Schottky barrier junctions, said rectifying Schottky barrier and essentially non-rectifying junctions each comprising a semiconductor and nonsemiconductor component;

b. electrically interconnecting a nonsemiconductor component of a member of the group consisting of: (the rectifying Schottky barrier drain (D) junction associated with said first semiconductor (100) channel region and the essentially non-rectifying source (S) junction associated with said first semiconductor (100) channel region), and, respectively, a member of the group consisting of: (the rectifying Schottky barrier drain (D) junction associated with said second semiconductor (100) channel region and the essentially non-rectifying source (S) junction associated with said second semiconductor (100) channel region);

c. electrically interconnecting said gates (G), such that during operation electrically noninterconnnected junctions are held at different voltages, and application of a gate voltage (Vg) controls effective semiconductor channel region doping type in both (MOSFET) devices, and thus which rectifying Schottky barrier drain (D) junction forward conducts and which does not forward conduct, thereby controlling the voltage present at the nonsemiconductor components of the electrically interconnected junctions essentially through said forward conducting rectifying semiconductor Schottky barrier drain (D) junction;
the basis of operation being that said Schottky barrier junctions are formed between said first and second semiconductor (100) channel regions and a material (108) which provides a rectifying junction to a semiconductor channel region when it is doped either N or P-type.

5. A Metal Oxide Semiconductor (MOS) device formed in a surface region of a semiconductor, comprising a Schottky barrier, (selected from the group consisting of rectifying and low reverse bias Schottky barrier potential effected essentially non-rectifying), to a semiconductor (100) channel region junction, wherein a gate (G) to which semiconductor (100) channel region doping type controlling voltage (Vg) can be applied is associated with said semiconductor (100) channel region and offset therefrom by insulating material (102), such that during use application of a sufficient negative voltage (Vg) to said gate (G) will cause attraction of holes into said semiconductor (100) channel region, and such that application of sufficient positive voltage (Vg) to said gate (G) will cause attraction of electrons into said semiconductor channel (100) region, the purpose of applying such gate voltage (Vg) being to modulate the doping type of said semiconductor (100) channel region; said Schottky barrier junction being formed in a region etched into said semiconductor, which etched region is partially comprised of insulating material (102), the purpose thereof being to reduce leakage current by limiting the area of Schottky barrier junction in contact with said semiconductor to a region near an end of said semiconductor (102) channel region.

6. A Metal Oxide Semiconductor (MOS) device as in Claim 5 in which the etched region in said semiconductor is such

that the insulating material (102) by which the gate (G) is offset from the semiconductor (100) channel region is undercut thereby and in which said Schottky barrier junction is present only at the end of said semiconductor (100) channel region which is located under said gate (G) offsetting insulator material (102).

7. A Metal Oxide Semiconductor (MOS) device system allowing control of a monitored voltage, said system being selected from the group consisting of:

a. a non-inverting single (MOS) device comprising a semiconductor (100) channel region and two rectifying Schottky barrier to channel region junctions in a surface region of a single doping type semiconductor, said rectifying Schottky barrier to channel region junctions being separated by said semiconductor (100) channel region, wherein a gate (G) to which semiconductor (100) channel region doping type modulating voltage (Vg) can be applied is associated with said semiconductor (100) channel region, said gate (G) being offset from said semiconductor (100) channel region by an insulating material (102), said monitored voltage being accessed at a junction to said semiconductor (100) channel region;

b. a non-inverting single (MOS) device comprising first and second Schottky barrier rectifying channel region junctions in a surface region of a single doping type semiconductor, said first and second Schottky barrier rectifying channel region junctions being separated by first and second semiconductor (100) channel regions from electrically interconnected essentially non-rectifying channel region junctions, wherein first and second gates (G) to which semiconductor (100) channel region doping type effecting modulating gate voltage can be applied are associated with said first and second semiconductor channel regions, said first and second gates (G) being offset from said first and second semiconductor (100) channel regions, respectively, by insulating material (102), said monitored voltage being accessed at a junction (M) to the electrically interconnected essentially non-rectifying Schottky barriers at a location between said first and second channel regions; and

c. an inverting single (MOS) device comprising first and second essentially non-rectifying channel region junctions in a surface region of a single doping type semiconductor, said first and second essentially non-rectifying channel region junctions being separated by first and second semiconductor (100) channel regions from electrically interconnected rectifying Schottky barrier to channel region junctions, wherein first and second gates (G) to which semiconductor (100) channel region doping type effecting modulating gate voltage (Vg) can be applied are associated with said first and second semiconductor (100) channel regions, said first and second gates being offset from said first and second semiconductor (100) channel regions, respectively, by insulating material (102), said monitored voltage being accessed at a junction (M) to the electrically interconnected rectifying Schottky barriers at a location between said first and second channel regions;

such that in use application of a positive polarity voltage (Vg) to a gate (G) causes an associated channel region to become effectively N-type by the attraction of electrons thereinto and application of a negative polarity voltage (Vg) to said gate (G) caused the channel region to become effectively P-type by attraction of holes thereinto, and such that a Schottky barrier to channel region junction is rectifying to said channel with either channel region effective doping present, but such that the direction of forward conduction through a rectifying Schottky barrier to channel region junction with effective N-type doping present is opposite to that with effective P-type doping present such that:

a. when a constant polarity voltage is applied between said first and second Schottky barrier junctions in said non-inverting single (MOS) device and said channel region effective doping is caused to switch from one effective doping type (N-type/P-type) to the other (P-type/N-type), by the changing of applied gate voltage (Vg) polarity, the monitored voltage present between said first and second Schottky barrier junctions changes from essentially that applied to one of said first and second Schottky barrier junctions to that applied to the other of said first and second Schottky barrier junctions, because of the reversal of forward conduction direction in said Schottky barrier to channel region junctions;

b. when a constant polarity voltage is applied between said first and second essentially non-rectifying channel region junctions in said inverting single (MOS) device, and said first and second channel regions effective doping is caused to switch from one effective doping type (N-type/P-type) to the other (P-type/N-type), by the changing of applied first and second gate voltage (Vg) polarity, the monitored voltage present at junction (M) to the electrically interconnected rectifying Schottky barrier junctions changes from essentially that applied to one of said first and second non-rectifying junctions to that applied to the other of said first and second non-rectifying junctions, because of the reversal of forward conduction direction in said Schottky barrier to channel region junctions.

8. A P(N)-Channel Schottky barrier MOSFET compring a device formed in a surface region of an N(P)-type Semiconductor, said P(N)-Channel MOSFET comprising two Schottky barrier junctions, termed Source (S) and Drain (D), which Source (S) and Drain (D) Schottky barrier junctions are separated by an N(P)-type Semiconductor (100) Channel region, in which P(N)-Channel Schottky barrier MOSFET a Gate (G) is offset from said N(P)-type Semiconductor (100) Channel Region by a region of insulator material (102), which P(N)-Channel Schottky barrier MOSFET provides significant Drain Current (ID) vs. Applied Drain (D) to Source (S) Voltage (VDS) as a function of Applied Gate Voltage (VG) Operating Curves only when the Voltage (VD) applied to the Drain (D) is of a Positive (Negative) Polarity, and when the Voltage (Vg) applied to the Gate (G) is of a Negative (Positive) Polarity so as to induce an inverted P(N)-type Channel Region, both said Applied Drain (VD) and Gate Voltages (Vg) being referenced to the Source (S) as a common terminal.

9. A Complementary Metal Oxide Semiconductor (CMOS) System which demonstrates regenerative switching in use, comprising an N-Channel Schottky barrier Metal Oxide Semiconductor Field Effect Transistor (MOSFET) in series combination with a P-Channel Schottky barrier MOSFET; which P-Channel Schottky barrier MOSFET comprises a device formed in a surface region of an N-type Semiconductor, said P-Channel MOSFET comprising two Schottky barrier junctions, termed Source (S) and Drain (D), which Source (S) and Drain (D) are separated by an N-type Semiconductor (100) Channel region, in which P-Channel Schottky barrier MOSFET a Gate (G) is offset from said N-type Semiconductor (100) Channel Region by a first region of insulator material (102), which P-Channel Schottky barrier MOSFET provides significant Drain (D) Current (ID) vs. Applied Drain to Source (S) Voltage (VD) as a function of Applied Gate Voltage (Vg) Operating Curves only when the Voltage (VD) applied to the Drain (D) is of a Positive Polarity, and when the Voltage (Vg) applied to the Gate (G) is of a Negative Polarity so as to induce an inverted P-type Channel Region, both said Applied Drain (VD) and Gate (Vg) Voltages being referenced to the Source (S) as a common terminal; and which N-Channel Schottky barrier MOSFET comprises a device formed in a surface region of a P-type Semiconductor, said N-Channel MOSFET comprising two Schottky barrier junctions, termed Source (S) and Drain (D), which Source (S) and Drain (D) are separated by a P-type Semiconductor (100) Channel region, in which N-Channel Schottky barrier MOSFET a Gate (G) is offset from said P-type Semiconductor (100) Channel Region by a second region of insulator material (102), which N-Channel Schottky barrier MOSFET provides significant Drain Current (ID) vs. Applied Drain junction to Source Voltage (VDS) as a function of Applied Gate Voltage (Vg) Operating Curves only when the Voltage (VD) applied to the Drain (D) is of a Negative Polarity, and when the Voltage (Vg) applied to the Gate (G) is of a Positive Polarity so as to induce an inverted N-type Channel Region, both said Applied Drain (VD) and Gate (Vg) Voltages being referenced to the Source (S) as a common terminal; the Source (S) of said N-Channel Schottky barrier MOSFET and the Source (S) of said P-Channel Schottky barrier MOSFET being electrically interconnected to one another, and said Gates (G) of said N and P-Channel Schottky Barrier MOSFETS being electrically interconnected to one another; such that when a Positive Polarity Voltage (VD) is applied to the electrically noninterconnected Drain (D) of the P-Channel Schottky barrier MOSFET, said Positive Polarity being with respect to the Voltage (VS) applied to the electrically noninterconnected Drain (D) of the N-Channel Schottky barrier MOSFET, and Voltage (Vg) at the electrically interconnected Gates (G) is set to essentially that applied to the electrically noninterconnected Drain (D) of the N-channel Schottky barrier MOSFET, the voltage (VM) at the electrically interconnected Sources (S) of the N and P-Channel Schottky barrier MOSFETS regeneratively switches to essentially that (VD) applied to the electrically noninterconnected Drain (D) of the P-Channel Schottky barrier MOSFET; and when the Voltage (Vg) at the electrically interconnected Gates (G) is set to essentially that applied to the electrically noninterconnected Drain (D) of the P-Channel Schottky barrier MOSFET, the voltage (VM) at the electrically interconnected Sources (S) regeneratively switches to essentially that (VS) applied to the electrically noninterconnected Drain of the N-Channel Schottky barrier MOSFET.

10. A Complementary Metal Oxide Semiconductor (CMOS) System which demonstrates regenerative switching in use as in Claim 9, in which the Semiconductor (100) is Silicon.

11. A Complementary Metal Oxide Semiconductor (CMOS) System which demonstrates regenerative switching in use as in Claim 10, in which the Source (S) and Drain (D) Schottky barrier junctions in both the N and P-Channel MOSFETS are formed between said Silicon (100) and at least one member of the group consisting of Chromium and Chromium Disilicide (108).

12. A method of configuring a Metal Oxide Semiconductor (MOS) gate voltage controlled rectification direction device and voltage controlled switch with operating characteristics similar to a non-latching Silicon Controlled Rectifier (SCR) comprising:

a. providing a (MOSFET) with a rectifying Schottky barrier first junction and a non-rectifying second junction in a surface region of a semiconductor (100), said first and second junctions being separated by a channel region in said semiconductor (100), said channel region having an insulator region (102) and gate (G) sequentially situated adjacent thereto;

b. applying a constant voltage between said second and first junctions of a polarity such that said rectifying Schottky barrier first junction is reverse biased, but conducts forward biased current if said second to first junction voltage polarity is reversed;

c. applying a gate (G) voltage (Vg) such that the channel region is caused to be inverted by the attraction of electrons thereto, thereby effecting a forward bias between said inverted channel region and said rectifying Schottky barrier first junction, such that forward biased current flows therethrough;
the basis of operation being that said Schottky barrier first junction is formed between said semiconductor (100) channel region and a material (108) which provides a rectifying junction to said semiconductor channel region when it is doped either N or P-type.

13. A semiconductor device comprising at least one Schottky barrier junction, said at least one Schottky barrier junction being formed from non-semiconductor and semiconductor components, which at least one Schottky barrier junction has as a non-semiconductor component a material which forms a rectifying junction with either N or P-type semiconductor, said semiconductor doping type being metalurgically or field induced.

14. A method of controlling a direction of rectification in a semiconductor device comprising the steps of :

(a) providing a device comprising at least one rectifying Schottky barrier junction, said at least one rectifying Schottky barrier junction being formed from non-semiconductor and semiconductor components, which at least one rectifying Schottky barrier junction has as a non-semiconductor component a material which forms a rectifying junction with either N or P-type semiconductor whether said semiconductor doping type is metalurgically or field induced, said semiconductor metalurgical doping type being selected from the group consisting of : (N-type, P-type and essentially Intrinsic);

(b) applying a voltage across said at least one rectifying Schottky barrier junction device;

(c) controlling the presence and direction of current flow through said Schottky barrier junction by application of a field which controls the effective doping type of said semiconductor.

15. A semiconductor system comprising at least one device selected from the group consisting of:

a. an inverting gate voltage channel induced semiconductor device with operating characteristics similar to multiple device Complimentary Metal Oxide Semiconductor (CMOS) systems, said inverting gate voltage channel induced semiconductor device being formed in a single doping type semiconductor and comprising two junctions, termed source and drain, which are separated by a first semiconductor channel region, and further comprising two additional junctions, termed source and drain, which are separated by a second semiconductor channel region, wherein gates, to which semiconductor channel region doping effecting voltage can be applied, are associated with each of the first and second semiconductor channel regions, said gates being offset from laid first and second semiconductor channel regions by insulating material; such that during use application a sufficient positive voltage to said gates will attract electrons to said first and second semiconductor channel regions, and such that application of sufficient negative voltage to said gates will attract holes to both of said first and second semiconductor channel regions, the purpose of applying such gate voltage being to modulate the effective doping type of said first and second semiconductor channel regions between respective source and drain junctions, which source junctions are each essentially non-rectifying, and which drain junctions are rectifying junctions;
in which inverting gate voltage channel induced semiconductor device the rectifying drain junction associated with said first semiconductor channel region is electrically interconnected with the rectifying drain junction associated with said second semiconductor channel region, and in which said gates associated with said first and second channel regions are electrically interconnected;
such that during operation the electrically noninterconnected essentially non-rectifying source junctions are held at different voltages, and application of a gate voltage controls effective semiconductor channel region doping type in both said first and second channel regions, and thus which electrically interconnected rectifying drain

junction forward conducts and which does not forward conduct, thereby controlling the voltage present at the electrically interconnected rectifying drain junctions essentially through said forward conducting rectifying drain junction;

b. a non-inverting gate voltage channel induced semiconductor device with operating characteristics similar to multiple device Complimentary Metal Oxide Semiconductor (CMOS) systems, said non-inverting gate voltage channel induced semiconductor device being formed in a single doping type semiconductor and comprising two junctions, termed source and drain, which are separated by a first semiconductor channel region, and further comprising two additional junctions, termed source and drain, which are separated by a second semiconductor channel region, wherein gates, to which semiconductor channel region doping effecting voltage can be applied, are associated with each of the first and second semiconductor channel regions, said gates being offset from said first and second semiconductor channel regions by insulating material; such that during use application a sufficient positive voltage to said gates will attract electrons to said first and second semiconductor channel regions, and such that application of sufficient negative voltage to said gates will attract holes to both of said first and second semiconductor channel regions, the purpose of applying such gate voltage being to modulate the effective doping type of said first and second semiconductor channel regions between respective source and drain junctions, which source junctions are each essentially non-rectifying, and which drain junctions are rectifying junctions;
in which non-inverting gate voltage channel induced semiconductor device the essentially non-rectifying source junction associated with said first channel region and the essentially non-rectifying source junction associated with the second channel region are electrically interconnected, and in which said gates associated with said first and second channel regions are electrically interconnected;
such that during operation the electrically non-interconncted rectifying drain junctions are held at different voltages, and application of a gate voltage controls effective semiconductor channel region doping type in both said first and second channel regions, and thus which electrically non-interconnected rectifying drain junction forward conducts and which does not forward conduct, thereby controlling the voltage present at the electrically interconnected essentially non-rectifying source junctions through said forward conducting rectifying drain junction;
the basis of operation of both the inverting and noninverting gate voltage channel induced semiconductor devices being that said rectifying drain junctions associated with said first and second semiconductor channel regions thereof are comprised of a material that forms a rectifying junction to a semiconductor channel region when it is doped either N or P-type by either metalurigical or field induced means; and

c. a non-inverting gate voltage channel induced semiconductor device with operating characteristics similar to multiple device Complimentary Metal Oxide Semiconductor (CMOS) systems, said non-inverting gate voltage channel induced semiconductor device being formed in a single doping type semiconductor and comprising two junctions, termed source and drain, which are separated by a semiconductor channel region, wherein a gate, to which semiconductor channel region doping effecting voltage can be applied, is associated with semiconductor channel region, said gate being offset from said semiconductor channel region by insulating material; such that during use application a sufficient positive voltage to said gate will attract electrons to said semiconductor channel region, and such that application of sufficient negative voltage to said gate will attract holes to said semiconductor channel region, the purpose of applying such gate voltage being to modulate the effective doping type of said semiconductor channel region between said source and drain junctions, which source and drain junctions are both rectifying junctions; said non-inverting gate voltage channel induced semiconductor device with operating characteristics similar to multiple device Complimentary Metal Oxide Semiconductor (CMOS) systems further comprising an electrical contact to said channel region;
such that during operation the rectifying source and drain junctions are held at different voltages, and application of a gate voltage controls effective semiconductor channel region doping type in said channel region, and thus which rectifying junction forward conducts and which does not forward conduct, thereby controlling the voltage present at the electrical contact to said channel region essentially through said forward conducting rectifying junction;
the basis of operation of said noninverting gate voltage channel induced semiconductor device being that said rectifying junctions associated with a semiconductor channel region are comprised of a material that forms a rectifying junction to semiconductor channel region when it is doped either N or P-type by either metalurigical or field induced means.

16. Inverting and non-inverting single device equivalents to dual device seriesed N and P-Channel MOSFETS CMOS systems; comprising two oppositely facing rectifying diodes in intrinsic, or a single doping type semiconductor,

wherein said rectifying diode direction of rectification changes depending upon what doping type, (N or P), be it metallurgically or field induced, is present in the semiconductor, said inverting and non-inverting single device equivalents to dual device seriesed N and P-Channel MOSFETS CMOS systems further comprising gate means for field inducing effective doping type in said semiconductor, and wherein a voltage monitored at an electrical contact between said rectifying diodes responds as a function of applied gate voltage, but is essentially electrically isolated therefrom.

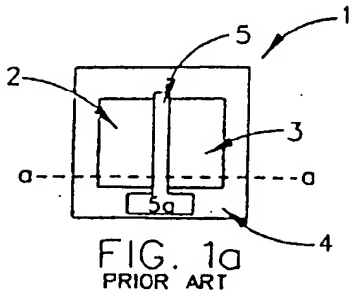

FIG. 1a
PRIOR ART

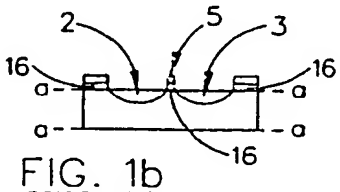

FIG. 1b
PRIOR ART

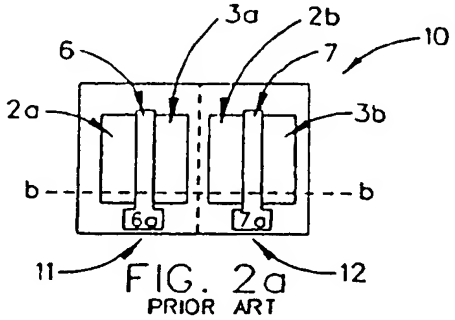

FIG. 2a
PRIOR ART

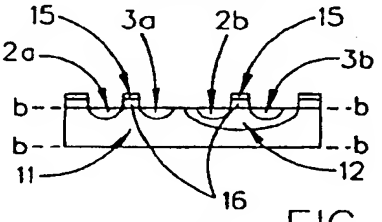

FIG. 2b
PRIOR ART

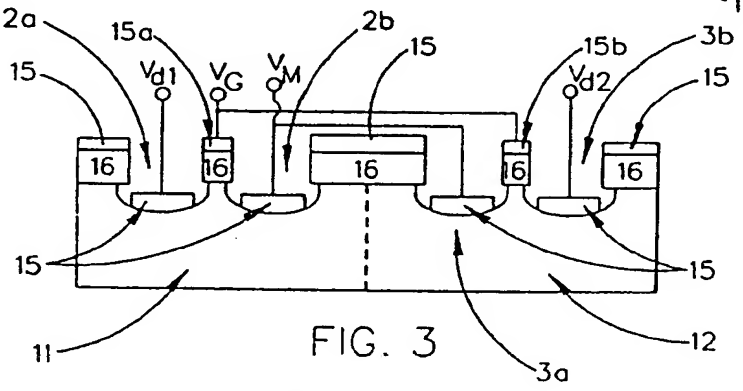

FIG. 3

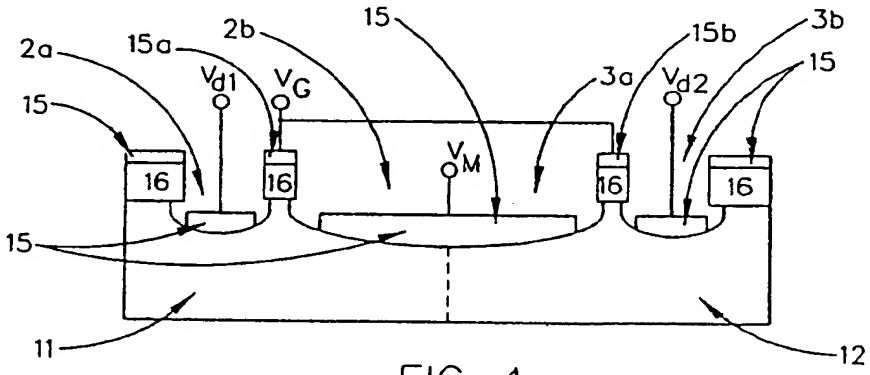

FIG. 4

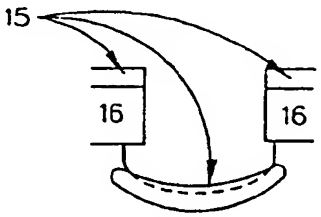

FIG. 5

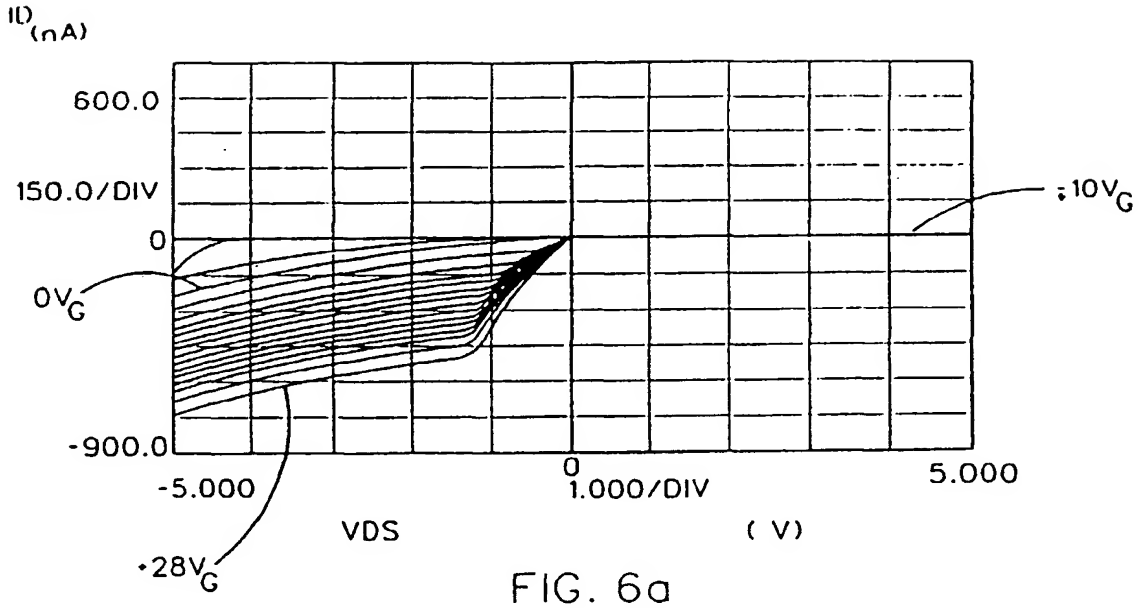

FIG. 6a

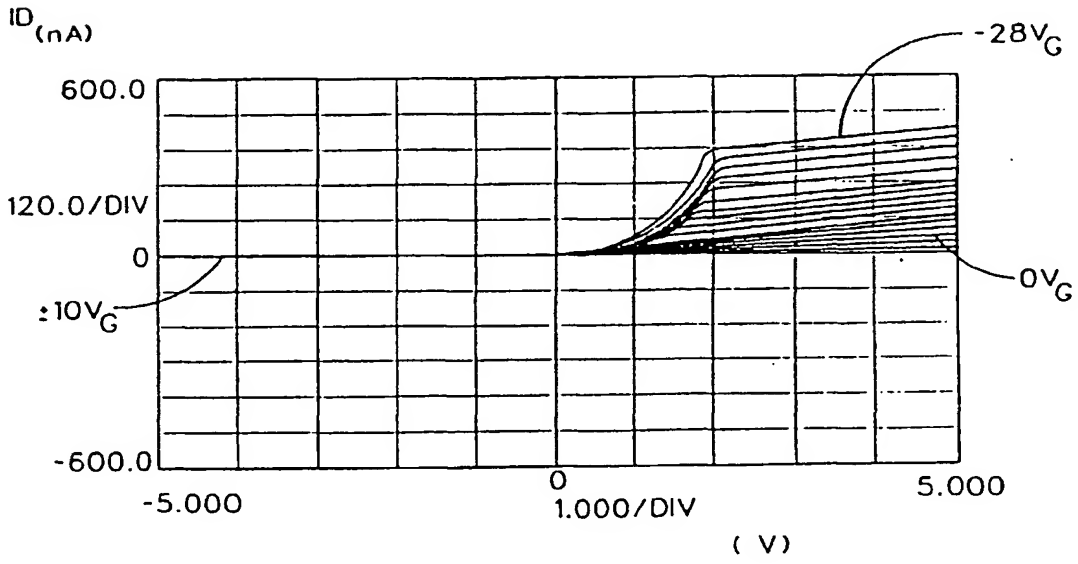

FIG. 7a

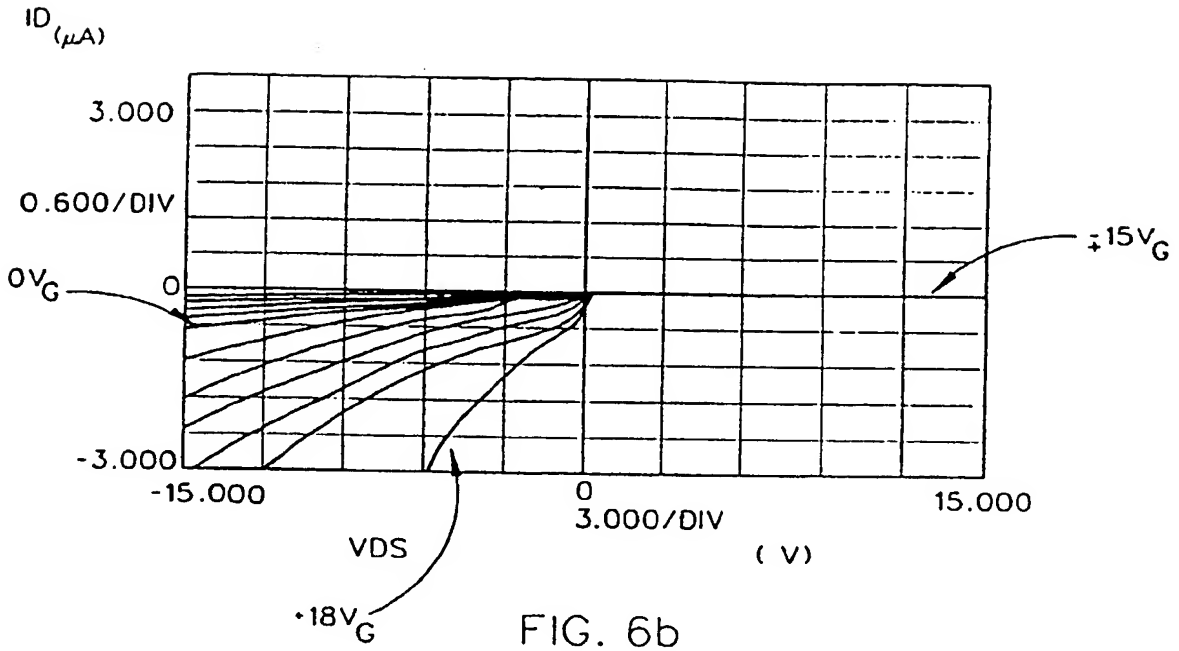

FIG. 6b

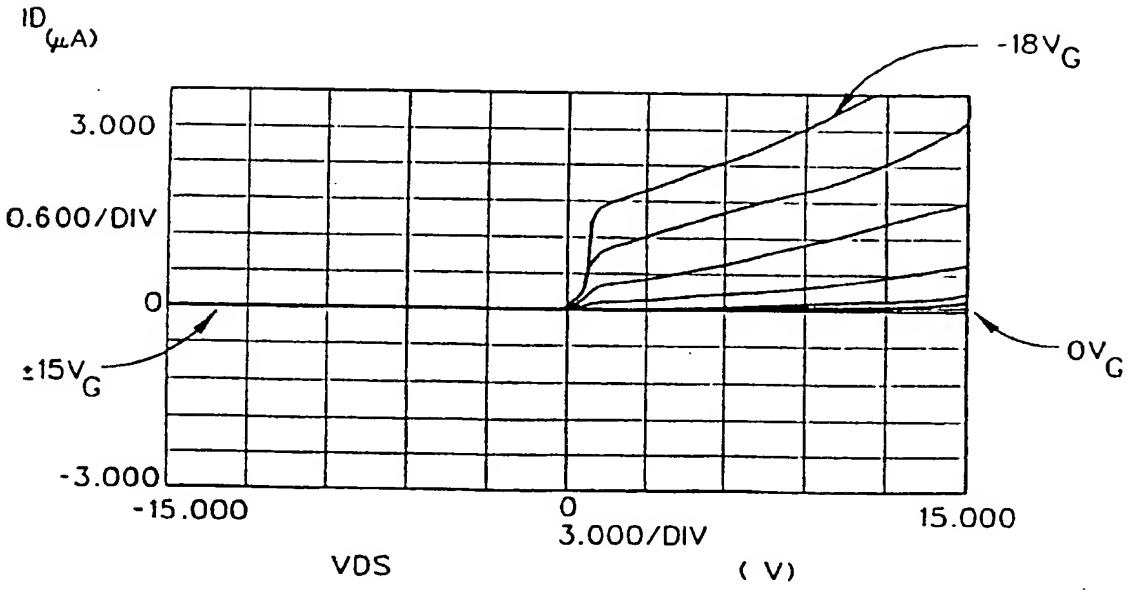

FIG. 7b

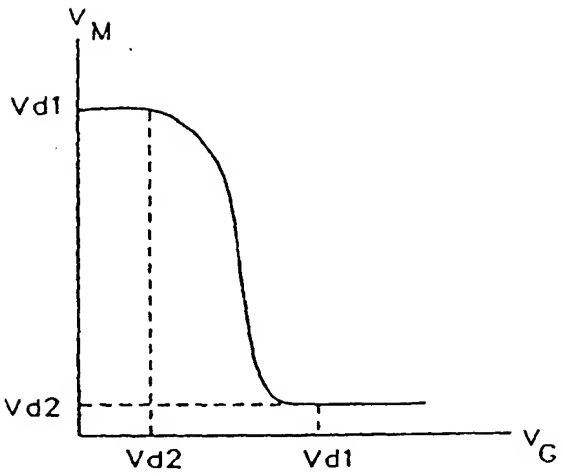

FIG. 8a

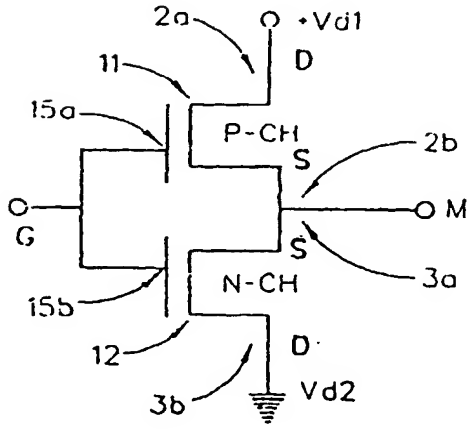

FIG. 8b

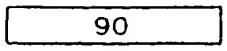

FIG. 9a

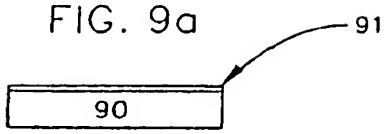

FIG. 9b

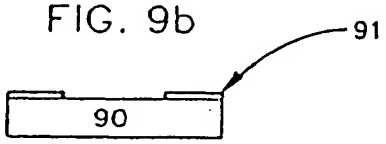

FIG. 9c

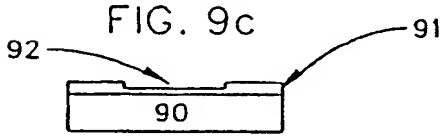

FIG. 9d

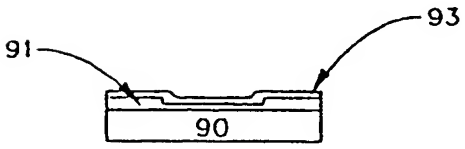

FIG. 9e

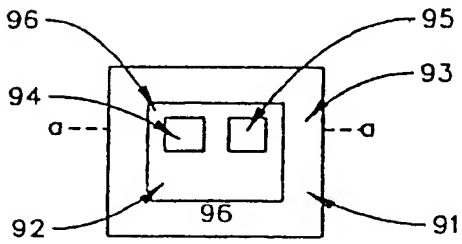

FIG. 9f

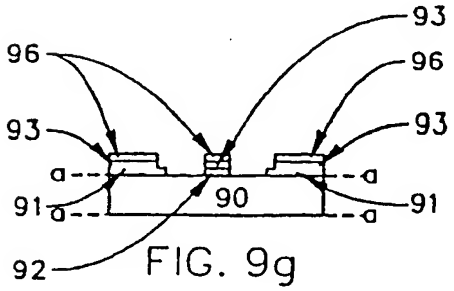

FIG. 9g

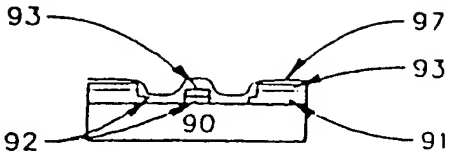

FIG. 9h

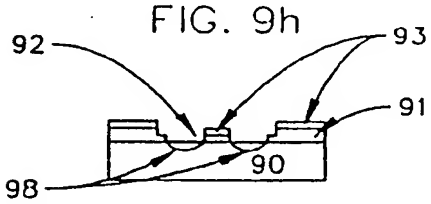

FIG. 9i

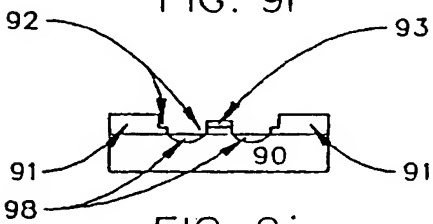

FIG. 9j

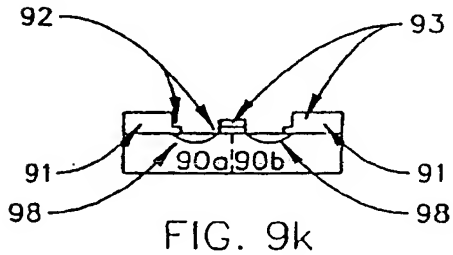

FIG. 9k

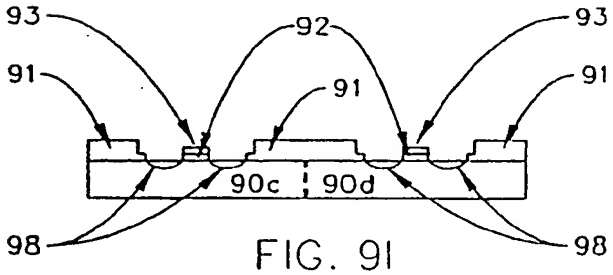

FIG. 9l

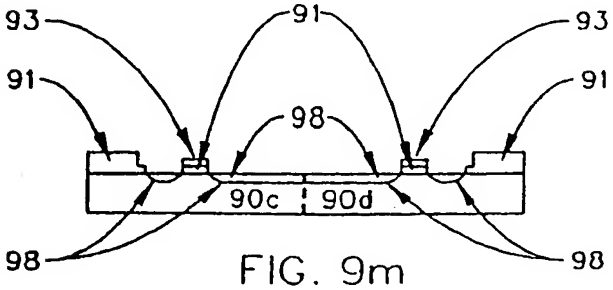

FIG. 9m

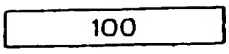

FIG. 10a

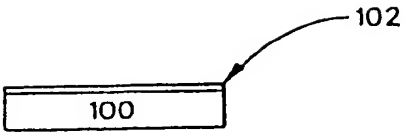

FIG. 10b

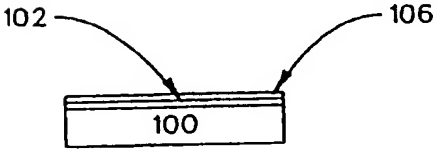

FIG. 10c

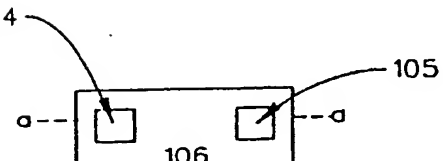

FIG. 10d

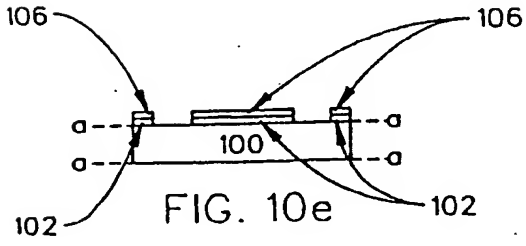

FIG. 10e

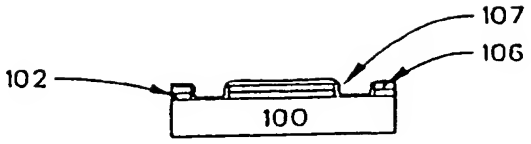

FIG. 10f

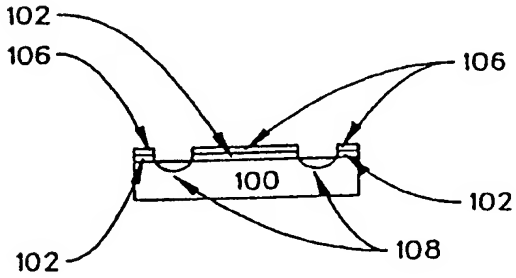

FIG. 10g

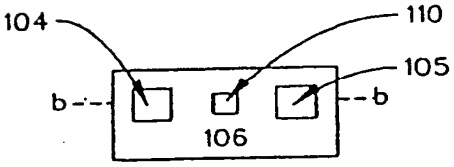

FIG. 10h

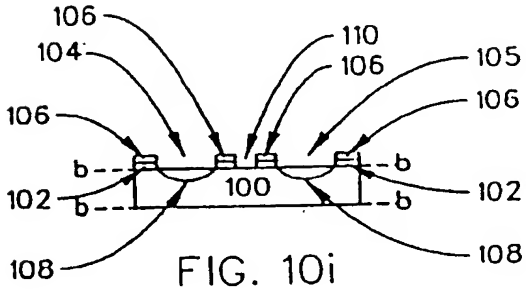

FIG. 10i

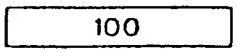

FIG. 10j

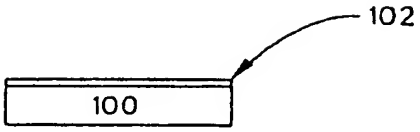

FIG. 10k

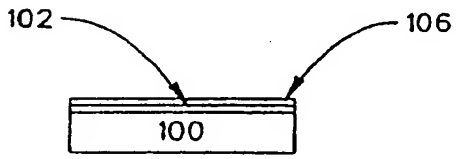

FIG. 10l

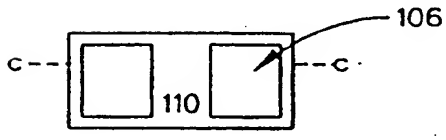

FIG. 10m

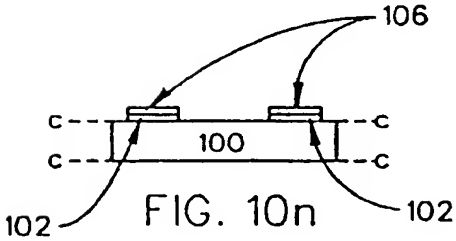

FIG. 10n

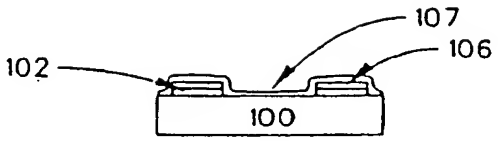

FIG. 10o

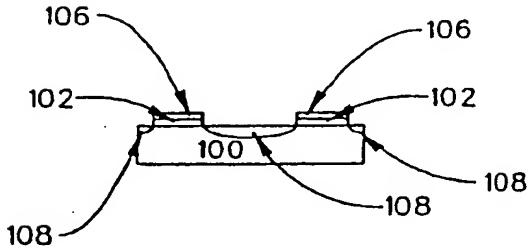

FIG. 10p

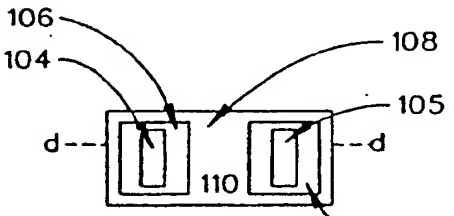

FIG. 10q

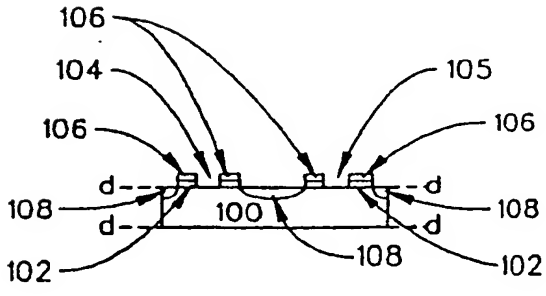

FIG. 10r

FIG. $11a_0$

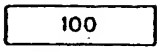

FIG. $11a_1$

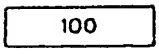

FIG. $11a_2$

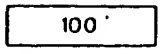

FIG. $11a_3$

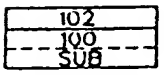

FIG. $11b_0$

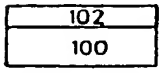

FIG. $11b_1$

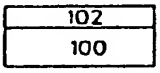

FIG. $11b_2$

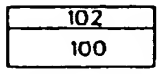

FIG. $11b_3$

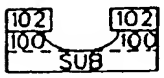

FIG. $11c_0$

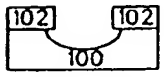

FIG. $11c_1$

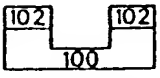

FIG. $11c_2$

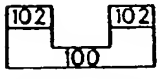

FIG. $11c_3$

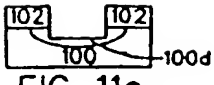

FIG. $11c_{3P}$

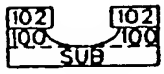

FIG. $11d_0$

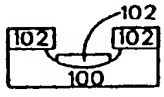

FIG. $11d_1$

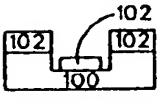

FIG. $11d_2$

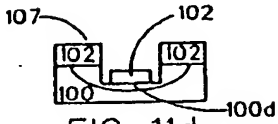

FIG. $11d_3$

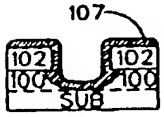

FIG. $11e_0$

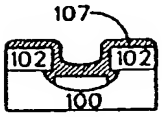

FIG. $11e_1$

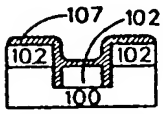

FIG. $11e_2$

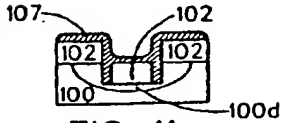

FIG. $11e_3$

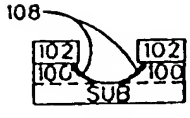

FIG. $11f_0$

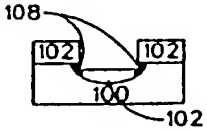

FIG. $11f_1$

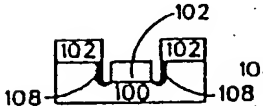

FIG. $11f_2$

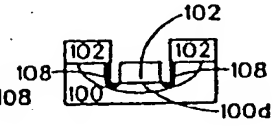

FIG. $11f_3$

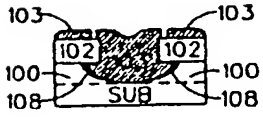

FIG. $11g_0$

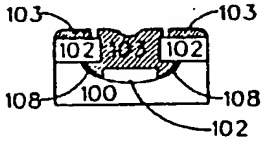

FIG. $11g_1$

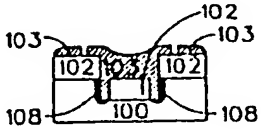

FIG. $11g_2$

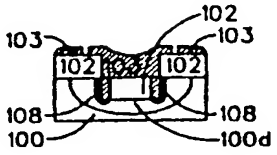

FIG. $11g_3$

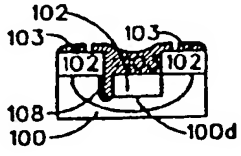

FIG. $11g_{3P}$

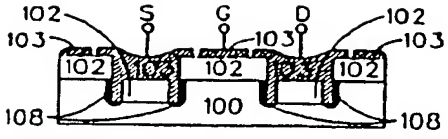

FIG. 11h$_a$

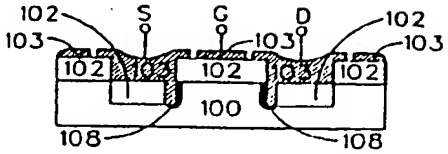

FIG. 11h$_b$

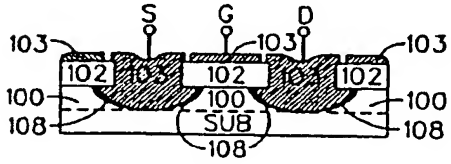

FIG. 11i

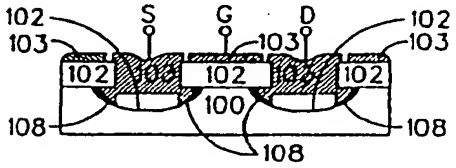

FIG. 11j

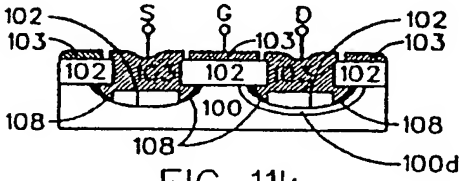

FIG. 11k

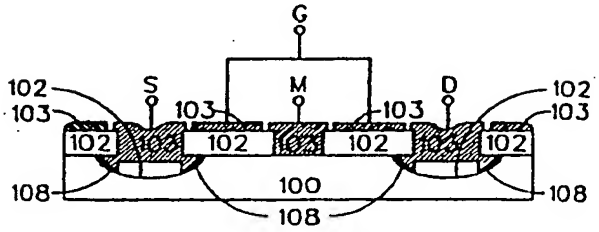

FIG. 11l

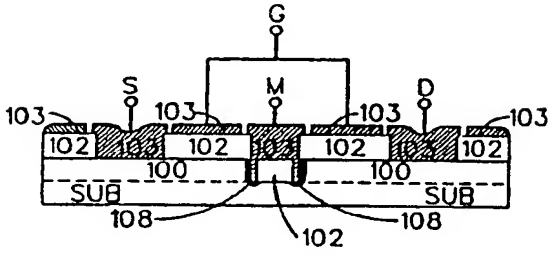

FIG. 11m

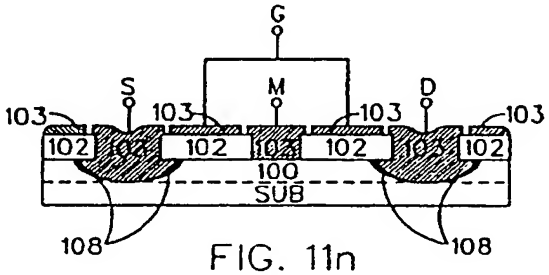

FIG. 11n

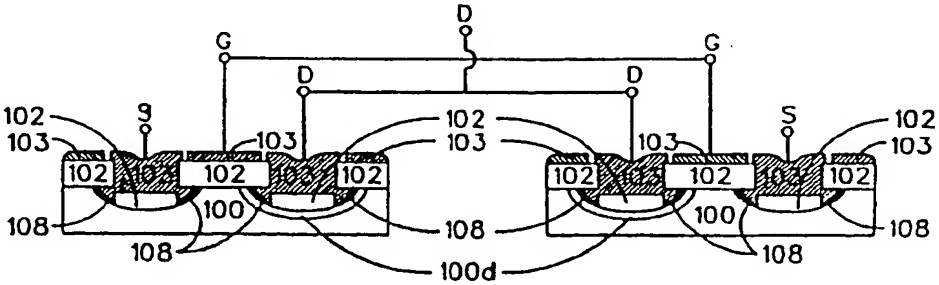

FIG. 11o

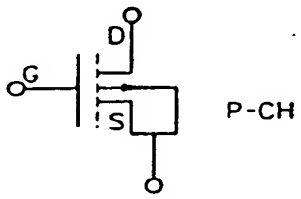

FIG. 12a

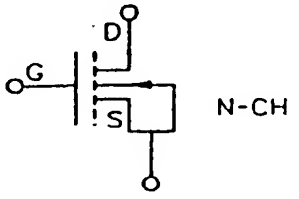

FIG. 12b

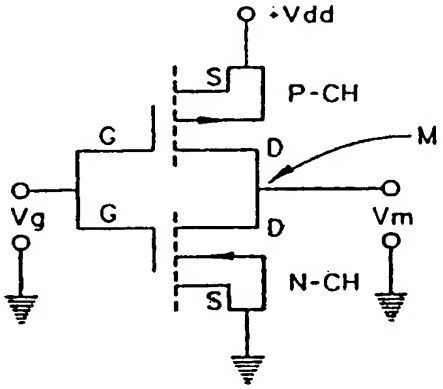

FIG. 13a

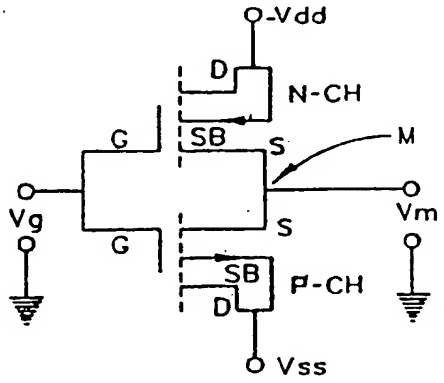

FIG. 13b

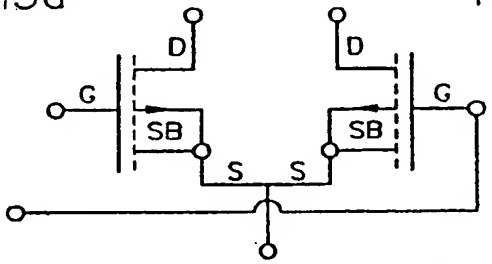

FIG. 14

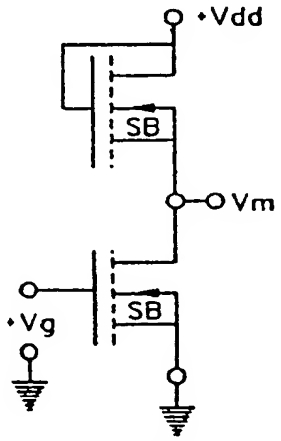

FIG. 15a

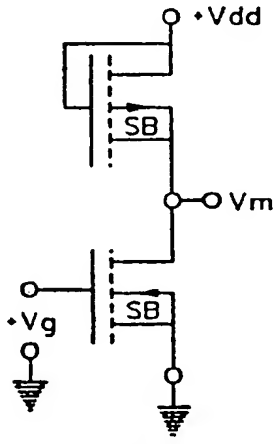

FIG. 15b

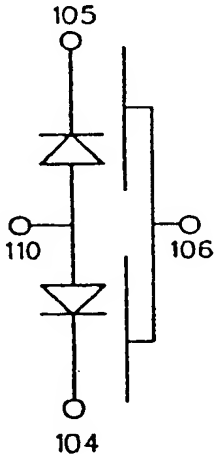

FIG. 16a

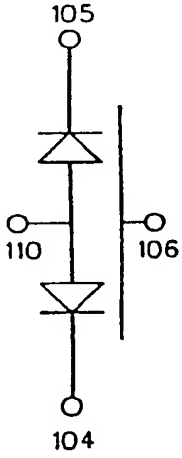

FIG. 16b

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 97 30 6688

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
X Y	PATENT ABSTRACTS OF JAPAN vol. 095, no. 006, 31 July 1995 & JP 07 066404 A (HITACHI LTD), 10 March 1995, * abstract; figures 4-14,31-36 *	5,6 1-4,8-12	H01L27/092
Y X	US 4 696 093 A (WELCH JAMES D) * column 2, line 39 - line 42 * * column 4, line 26 - line 43 * * abstract; claims; figures 1,2 *	1-4,8-12 13,14	
X	WO 86 01641 A (AMERICAN TELEPHONE & TELEGRAPH) * page 1, line 22 - line 33 * * page 8, line 1 - page 9, line 13 * * abstract; claims; figures 1-8 *	5,6	
X	PATENT ABSTRACTS OF JAPAN vol. 012, no. 435 (E-683), 16 November 1988 & JP 63 168046 A (NEC CORP), 12 July 1988, * abstract *	13,14	TECHNICAL FIELDS SEARCHED (Int.Cl.6) H01L
A	PATENT ABSTRACTS OF JAPAN vol. 009, no. 212 (E-339), 29 August 1985 & JP 60 074561 A (FUJITSU KK), 26 April 1985, * abstract *	1-4,8-14	

-/--

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	29 January 1998	Wirner, C

CATEGORY OF CITED DOCUMENTS

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D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document

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European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 97 30 6688

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
A	RISHTON S A ET AL: "New complimentary metal-oxide semiconductor technology with self-aligned Schottky source/drain and low-resistance T gates" 41ST INTERNATIONAL CONFERENCE ON ELECTRON, ION, AND PHOTON BEAMS TECHNOLOGY AND NANOFABRICATION, DANA POINT, CA, USA, 27-30 MAY 1997, vol. 15, no. 6, ISSN 0734-211X, JOURNAL OF VACUUM SCIENCE & TECHNOLOGY B (MICROELECTRONICS AND NANOMETER STRUCTURES), NOV.-DEC. 1997, AIP FOR AMERICAN VACUUM SOC, USA, pages 2795-2798, XP002053150 * page 2797, column 1, line 15 - column 2, line 10; figure 5 * ---	1,5,7-9, 12-14	
A	US 5 164 812 A (HALL JOHN H) * abstract; claims; figure 2 * * column 2, line 13 - column 3, line 4 * ---	1,5	
E	US 5 663 584 A (WELCH JAMES D) * the whole document * -----	1-14	TECHNICAL FIELDS SEARCHED (Int.Cl.6)

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	29 January 1998	Wirner, C

CATEGORY OF CITED DOCUMENTS

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A : technological background
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E : earlier patent document, but published on, or after the filing date
D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document

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